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Introduction to Digitally Assisted Analog and RF Circuit Design

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Matsuzawa & Okada Lab.

Contents

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- **Tradeoffs in analog: area, cost, mismatch, power consumption, and response;**

  Solution by DAA in DAC

- **Power consumption and mismatch in analog**

  Solution by DAA in ADC

- **Not robust and programmable in analog**

  Solution by DAA in RF-CMOS Tuner

DAA: Digitally Assisted Analog technology

“Digitally Assisted Analog and RF Design”

- **What is “Digitally Assisted Analog and RF Design”**

  To use digital technology for analog and RF circuits as much as possible to solve analog issues.

- **Why digital technology is needed…?**
  - **Digital is more robust and programmable**
  - **Digital is more power efficient**
  - **Digital is cheaper and low power in scaled CMOS**

- **Will analog go out?**
  - **No, important forever, however needs assists by digital**

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Tradeoff:
Area, cost, mismatch, power dissipation, and response

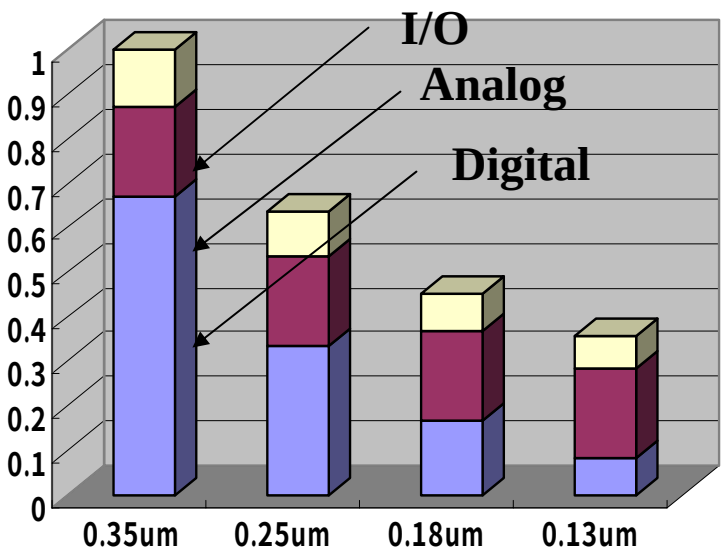
The nature of analog and breakthrough by digital assistance

Example: DAC

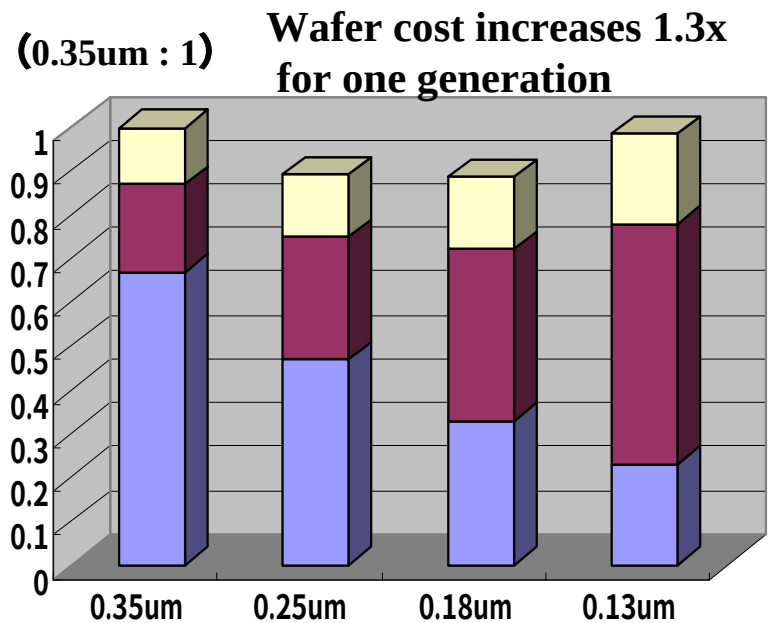
Cost up issue by analog parts in scaled CMOS

Cost of mixed A/D LSI will increase with technology scaling, due to the increase of cost in non-scalable analog.

Large analog must be unacceptable.



Chip area



Chip cost

Akira Matsuzawa, “RF-SoC- Expectations and Required Conditions,”
IEEE Tran. On Microwave Theory and Techniques, Vol. 50, No. 1, pp. 245-253, Jan. 2002

Technology trend in RF CMOS LSI

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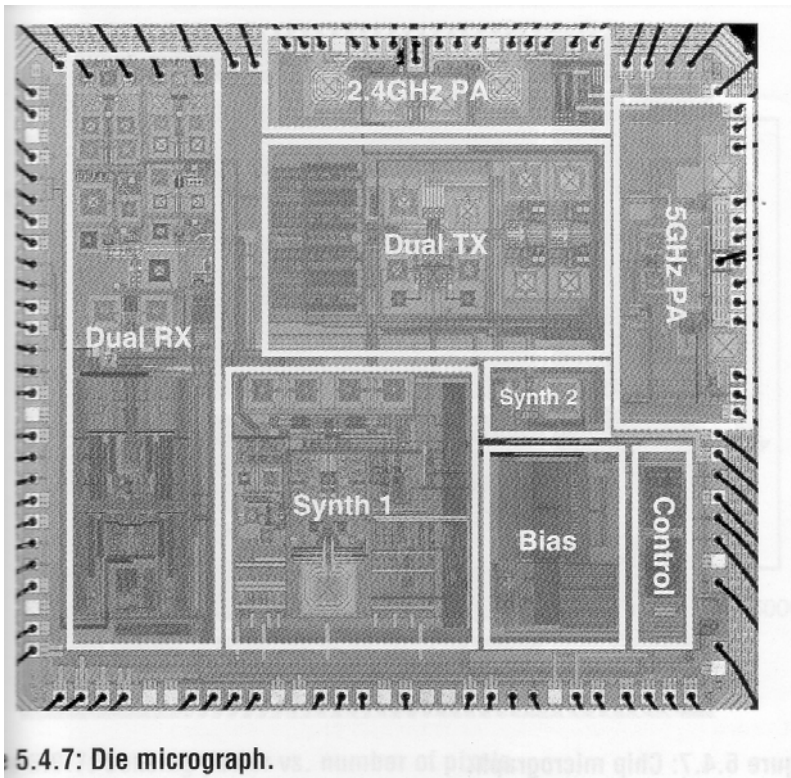
Analog & RF CMOS will be replaced by Digitally assisted RF CMOS.

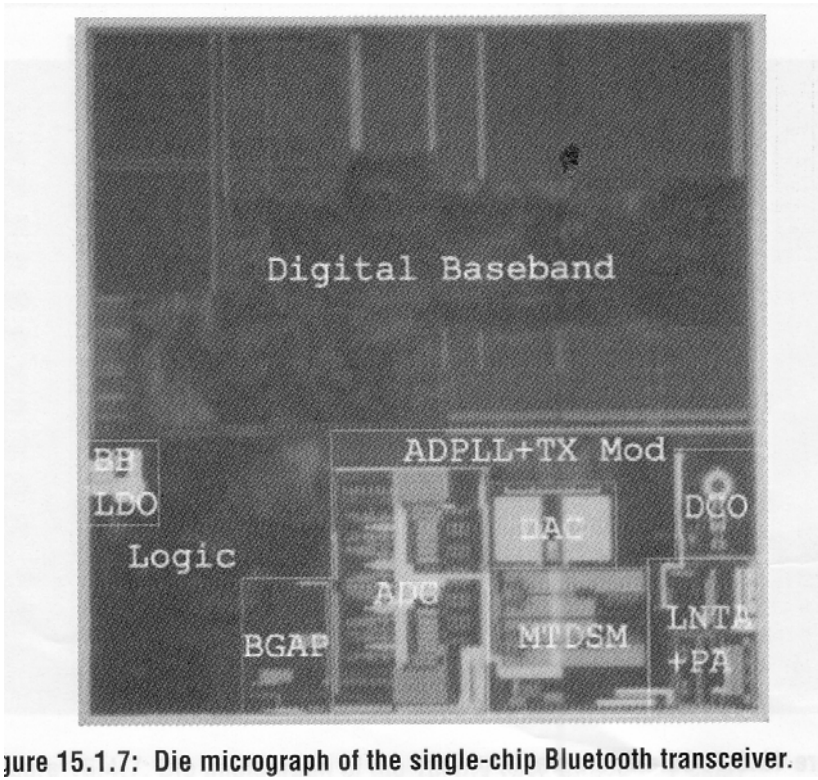
Wireless LAN, 802.11 a/b/g
0.25um, 2.5V, 23mm^2, 5GHz



5.4.7: Die micrograph.

M. Zargari (Atheros), et al., ISSCC 2004, pp.96

Discrete-time Bluetooth
0.13um, 1.5V, 2.4GHz



ure 15.1.7: Die micrograph of the single-chip Bluetooth transceiver.

K. Muhammad (TI), et al., ISSCC2004, pp.268

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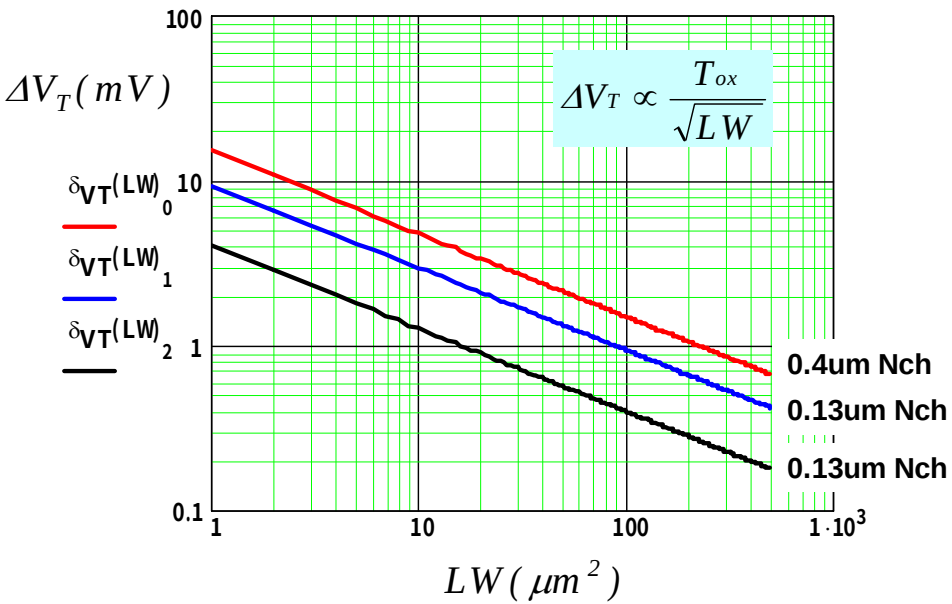
Nature of analog: Mismatch and area

Mismatch of analog components is inversely proportional to squire root of area.

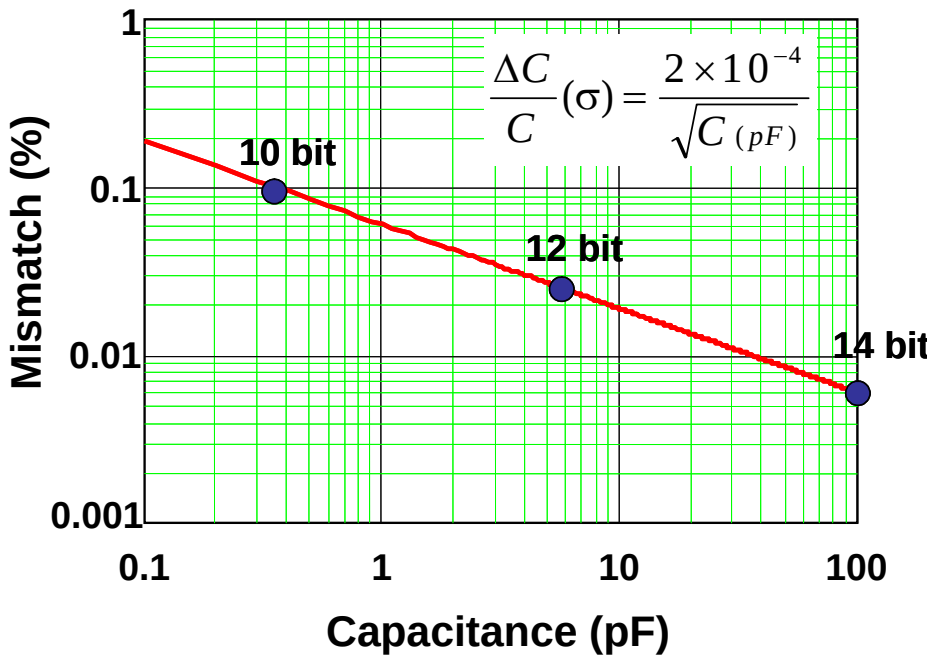
Thus accuracy and performance and cost in analog circuits always trade off.

$$Mismatch \propto \frac{1}{\sqrt{Area}}$$

V_T mismatch vs. gate size



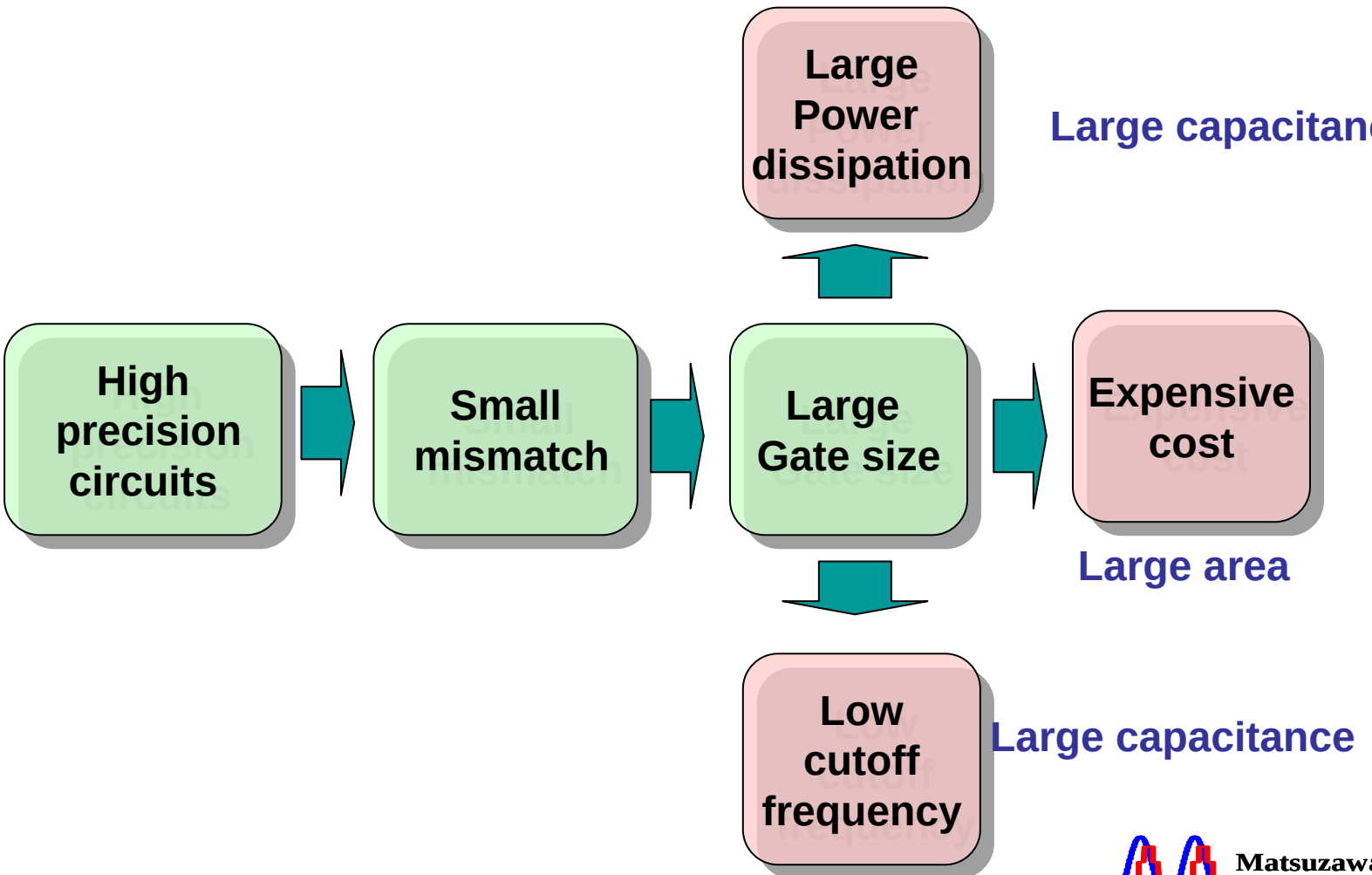
Capacitor mismatch vs. capacitance



Essential issue in analog technology

To realize high precision circuits always increases power dissipation and area & cost and decreases frequency performance.

The digital assistance can solve this essential issue of analog.



Pioneer work in digital assistance

Conventionally large area is required to realize high precision DAC, such 14 bit. However this results in increase of power and degrade frequency characteristics.

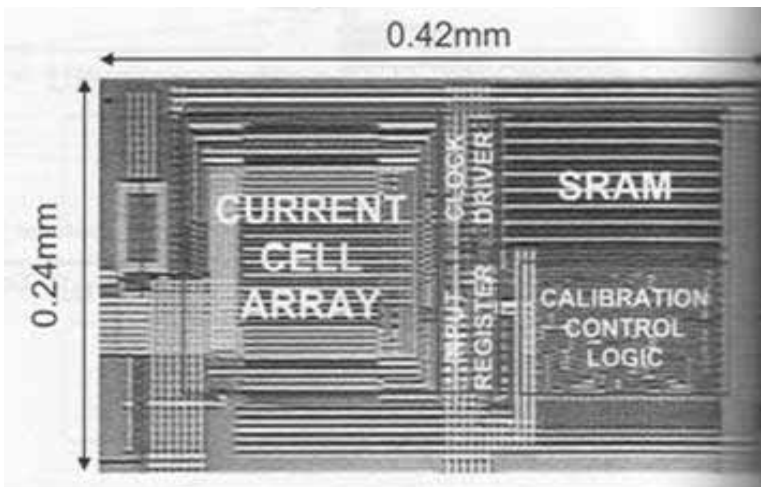
Iowa university demonstrated extremely small area and power can be realized by digital calibration.

14b 100MS/s DAC

1.5V, 17mW, 0.1mm^2, 0.13um

SFDR=82dB at 0.9MHz, 62dB at 42.5MHz

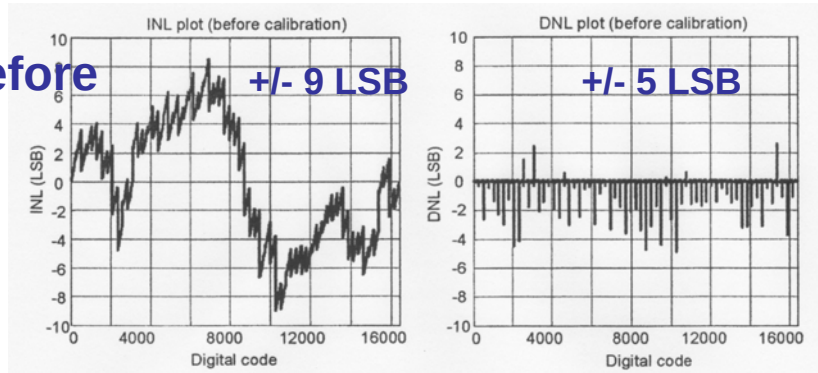
Area: 1/50 **Pd: 1/20**



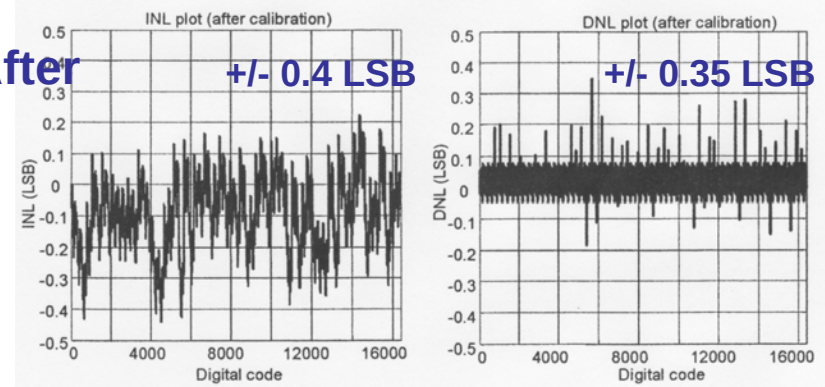
Y. Cong and R. L. Geiger, Iowa state university, ISSCC 2003

INL **DNL**

Before



After



14bit DAC

Architecture of digitally compensated DAC

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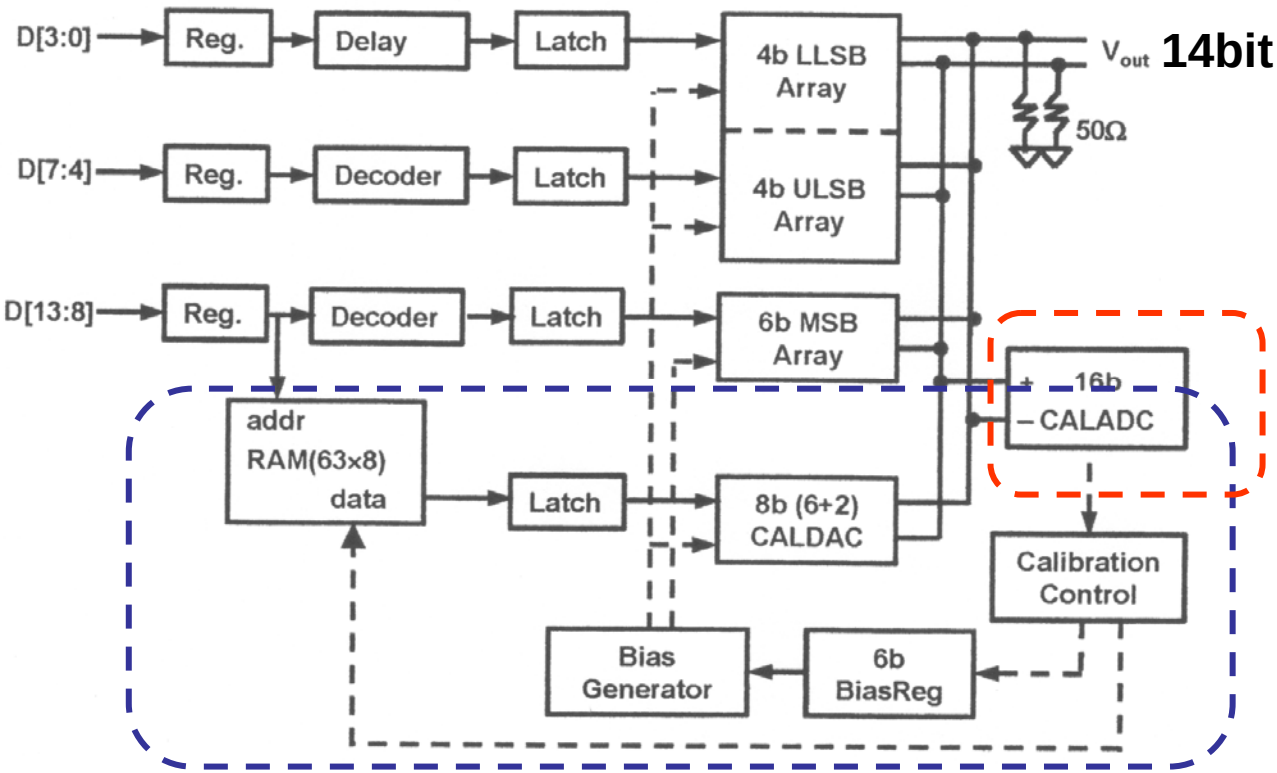
External ADC measure the nonlinearity and CAL DAC compensates it.

An idea is excellent, but the implementation (needs ADC) is not smart.



14bit 100MHz DAC

Y. Cong and R. L. Geiger,
Iowa state university, ISSCC 2003

Our developed 14b DAC without ADC

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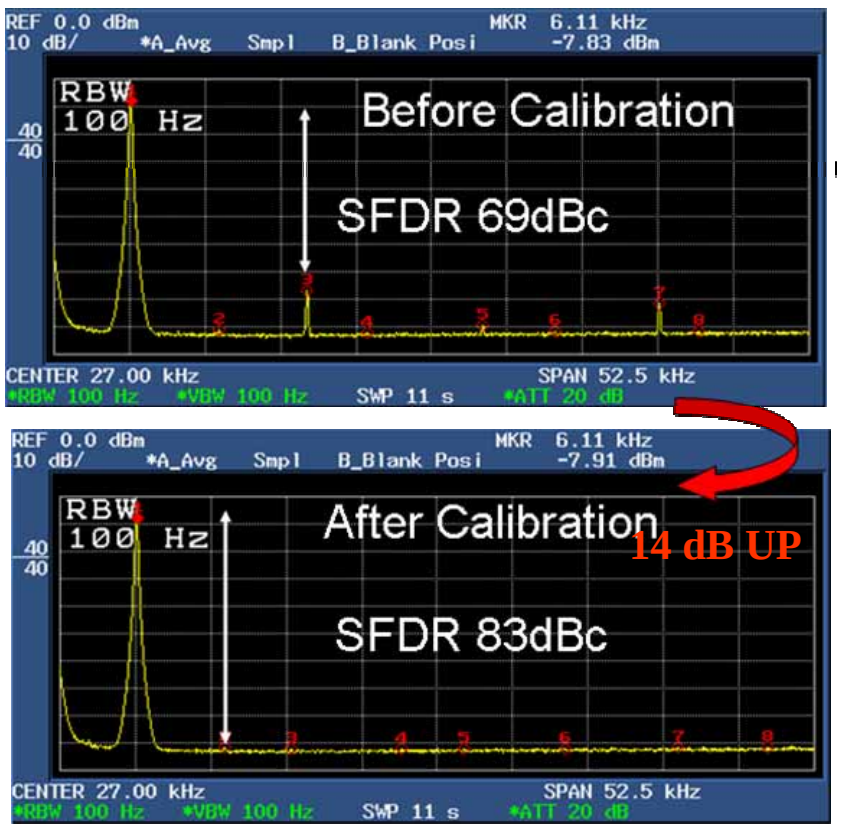
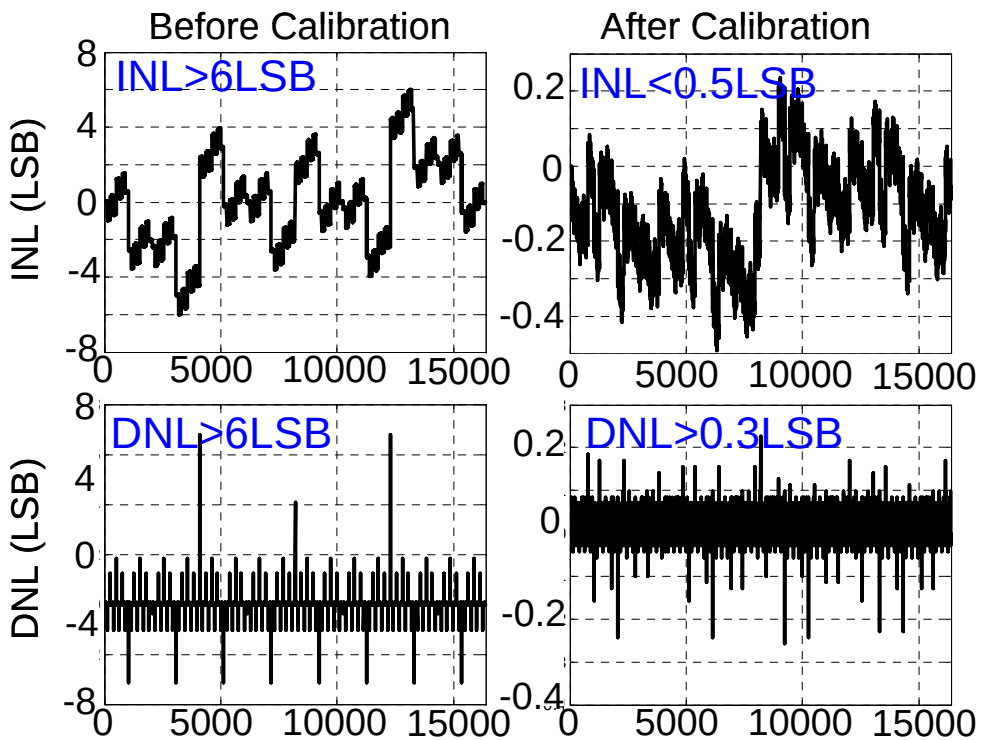
We developed 14b digitally calibrated DAC without ADC for error measurement.

Good SFDR of 83dB has been attained in spite of bare SFDR is 69 dB.

Yusuke Ikeda, Matthias Frey, and Akira Matsuzawa
A-SSCC, 13-3, pp 356-359, Korea, Jeju, Nov, 2007.





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Method for compensation

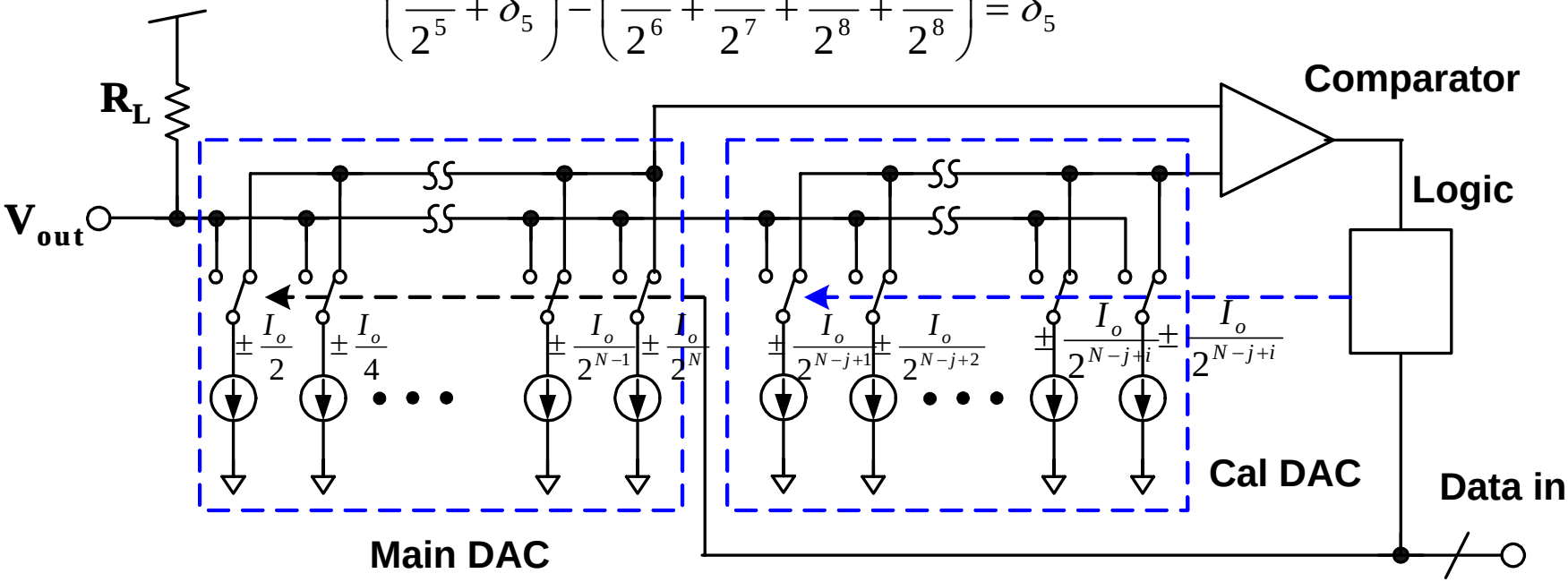
Only comparator and cal DAC are required to extract linearity error.

Nature of binary weighted values

$$\frac{1}{2^m} = \sum_{n=1}^{i} \frac{1}{2^{m+n}} + \frac{1}{2^{m+i}} \qquad \frac{1}{2^5} = \frac{1}{2^6} + \frac{1}{2^7} + \frac{1}{2^8} + \frac{1}{2^8}$$

The error can be extracted by comparing two values and balanced with CAL DAC

$$\left(\frac{1}{2^5} + \delta_5\right) - \left(\frac{1}{2^6} + \frac{1}{2^7} + \frac{1}{2^8} + \frac{1}{2^8}\right) = \delta_5$$



Calibration pass and chip photograph

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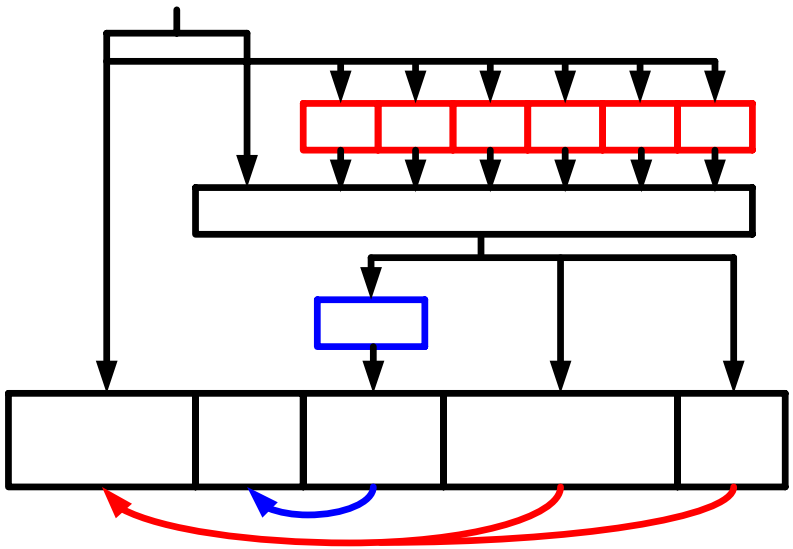
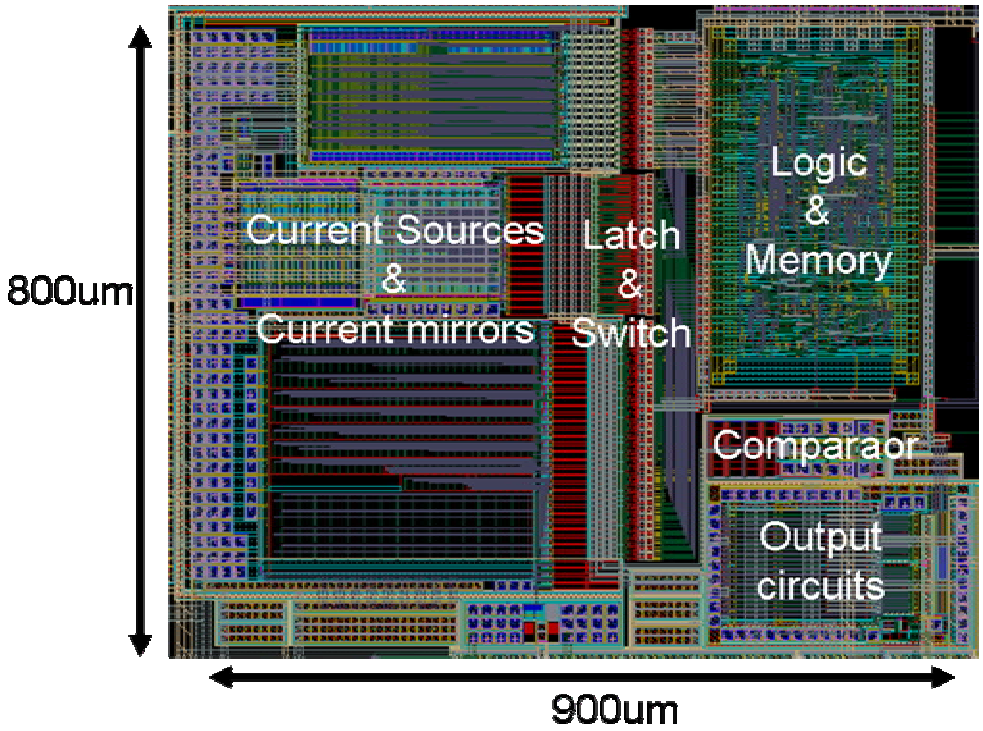
Extracted errors is stored in registers and used for compensation digitally.

Yusuke Ikeda, Matthias Frey, and Akira Matsuzawa
A-SSCC, 13-3, pp 356-359, Korea, Jeju, Nov, 2007.



In[13:0]

In[13:8]



[13] [12] [11] [10] [9] [8]

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OPamp-base design to comparator-base design

Conventional analog circuits consume static current

Low power dissipation by digital assistance

Example: ADC

Issues of pipeline ADCs

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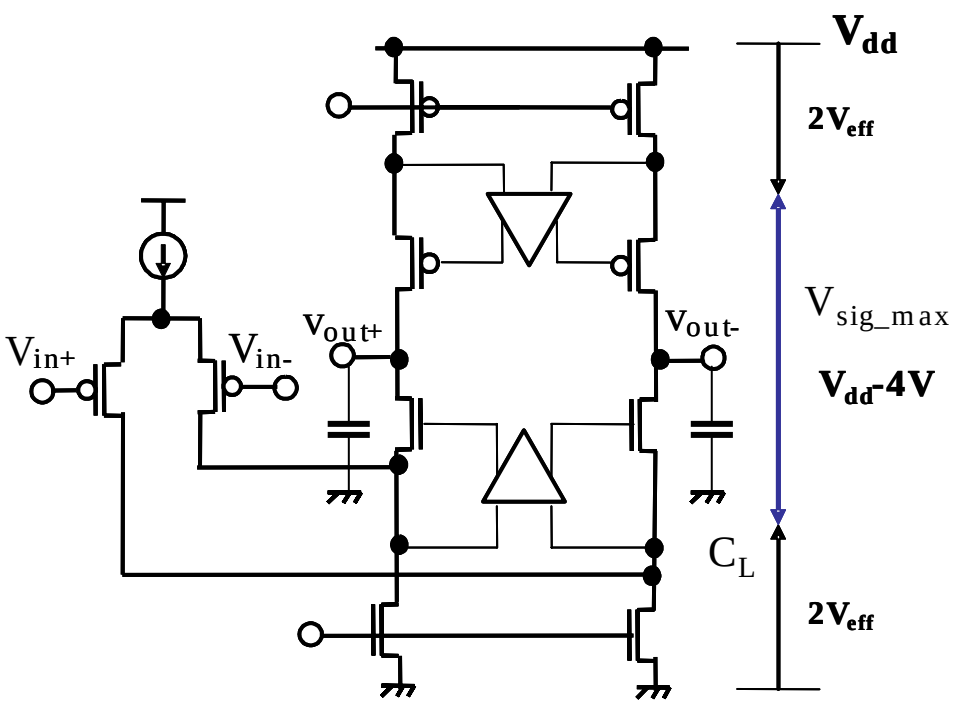
Major issues of pipeline ADCs are caused by OpAmp.

High OPamp gain is required for high precision ADC, however it becomes quite difficult with technology scaling.

$$G_{DC}(dB) > 6N + 10$$

$$10b : 70dB$$

$$12b : 82dB$$

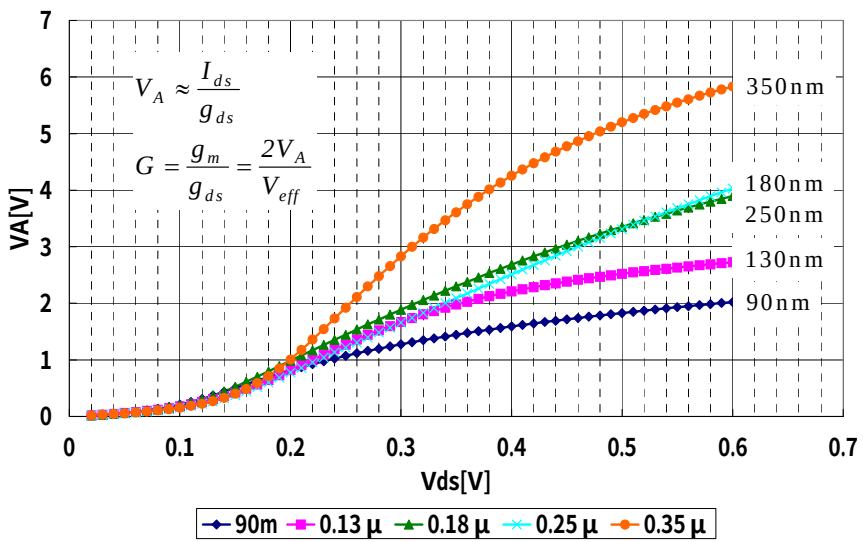


Sub-100nm CMOS

$$G_{DC} \approx \left(\frac{V_A}{V_{eff}}\right)^n \approx \left(\frac{1}{0.15}\right)^n \approx 16dB \times n$$

$$n < 5$$

$$G_{DC} < 80dB$$



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Conversion speed of pipeline ADC

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Speed of pipeline ADC is proportional to the OPamp current basically.

$$f_c \approx \frac{3GBW_{\_close}}{N} \propto \frac{I_{ds}\beta(I_{ds})}{C_L(I_{ds})}$$

$$GBW_{\_close} = \frac{g_m \cdot \beta}{2\pi C_L} = \frac{g_m}{2\pi C_o} \frac{1}{\left(2+\frac{C_{pi}}{C_o}\right)\left(1+\frac{C_{po}}{C_o}\right)+\left(1+\frac{C_{pi}}{C_o}\right)}$$

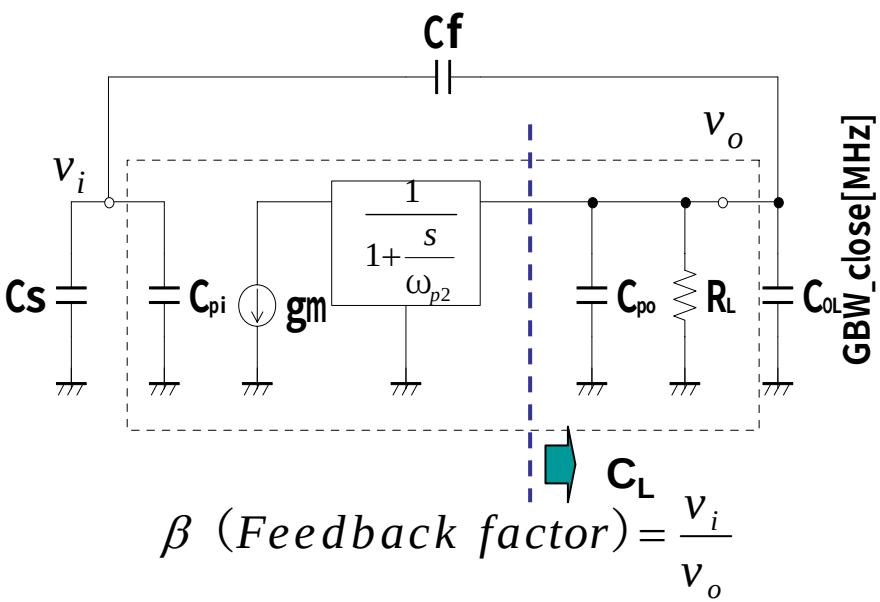
$$= \frac{I_{ds}}{\pi C_o V_{eff}} \frac{1}{\left(2+\frac{\alpha_{pi} I_{ds}}{C_o}\right)\left(1+\frac{\alpha_{po} I_{ds}}{C_o}\right)+\left(1+\frac{\alpha_{pi} I_{ds}}{C_o}\right)}$$

A. Matsuzawa, “Analog IC Technologies for Future Wireless Systems,” IEICE, Tan on Electronics, Vol. E89-C, No.4, pp. 446-454, April, 2006.

$$g_m = \frac{2I_{ds}}{V_{eff}}$$

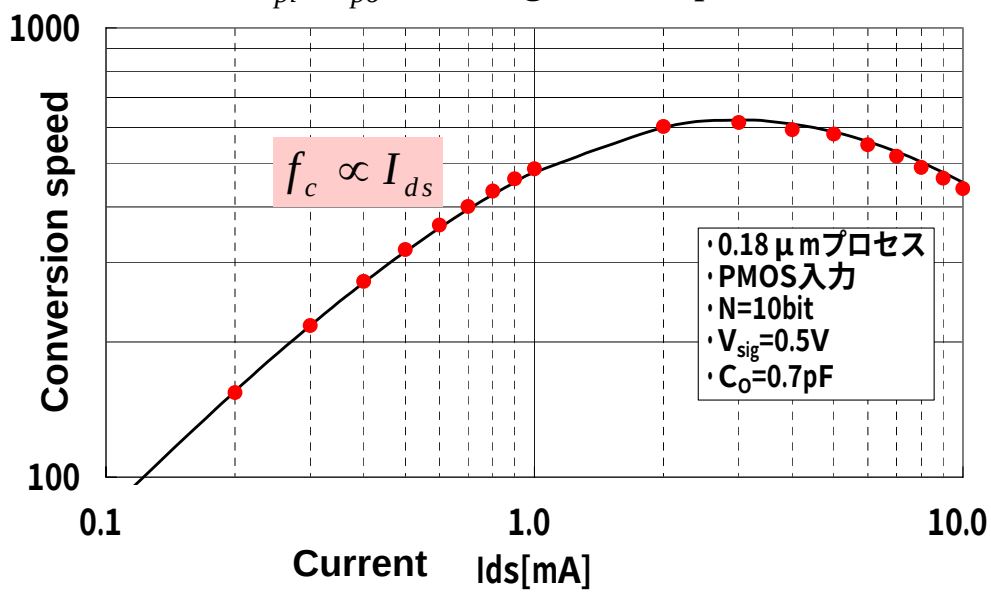
$$C_{pi} = \alpha_{pi} I_{ds}, \quad C_{po} = \alpha_{po} I_{ds}$$

Performance model



$$\beta\ (Feedback\ factor) = \frac{v_i}{v_o}$$

α_{pi}, α_{po} are design rule dependent



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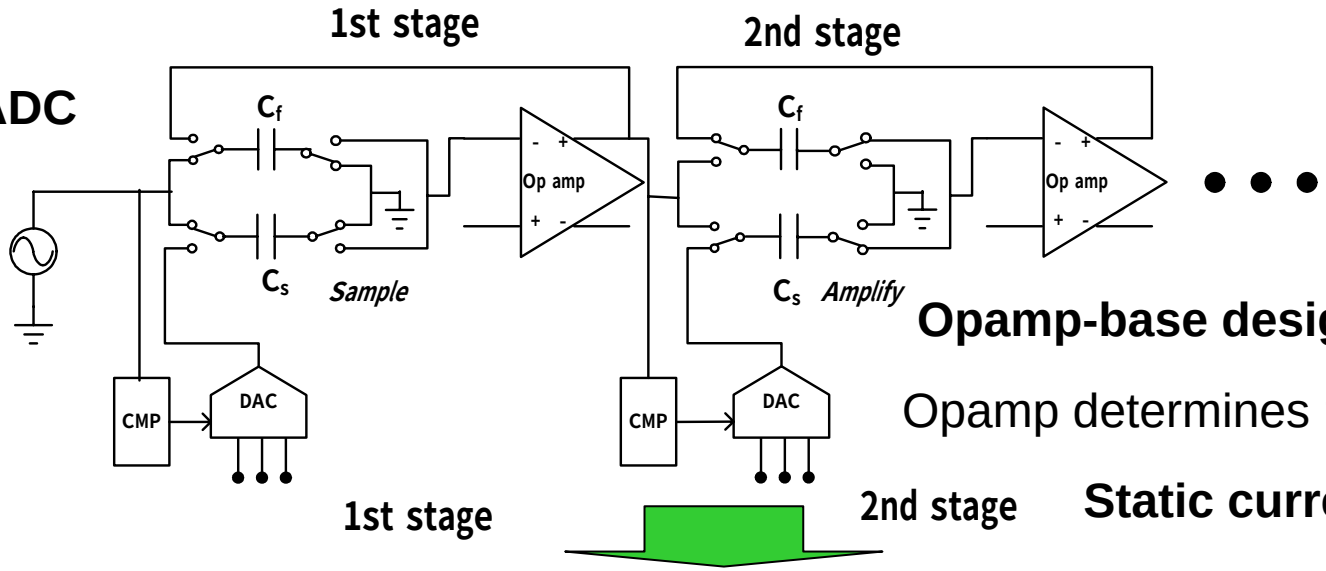
Mega-technology trend in ADCs

A major conversion scheme of ADCs is now changing from pipeline to SA

Pipeline ADC

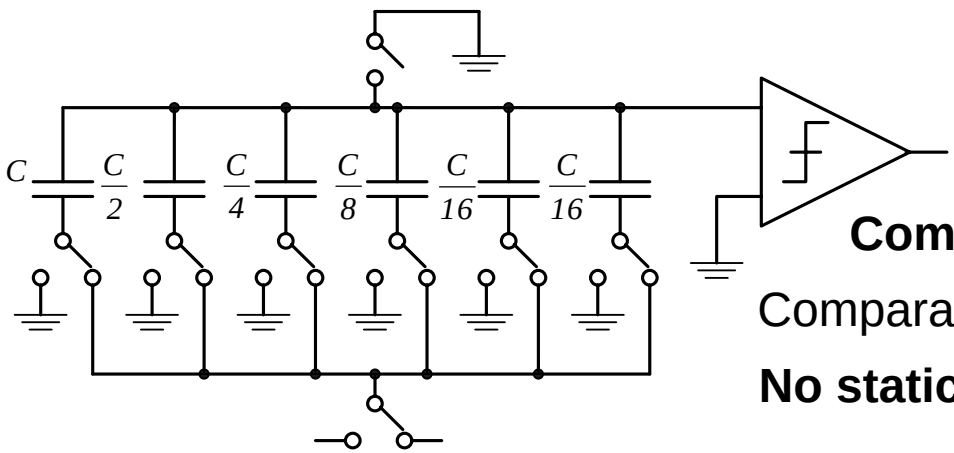


Opamp-base design

Opamp determines performance

Static current flows

SA ADC



Comparator-base design

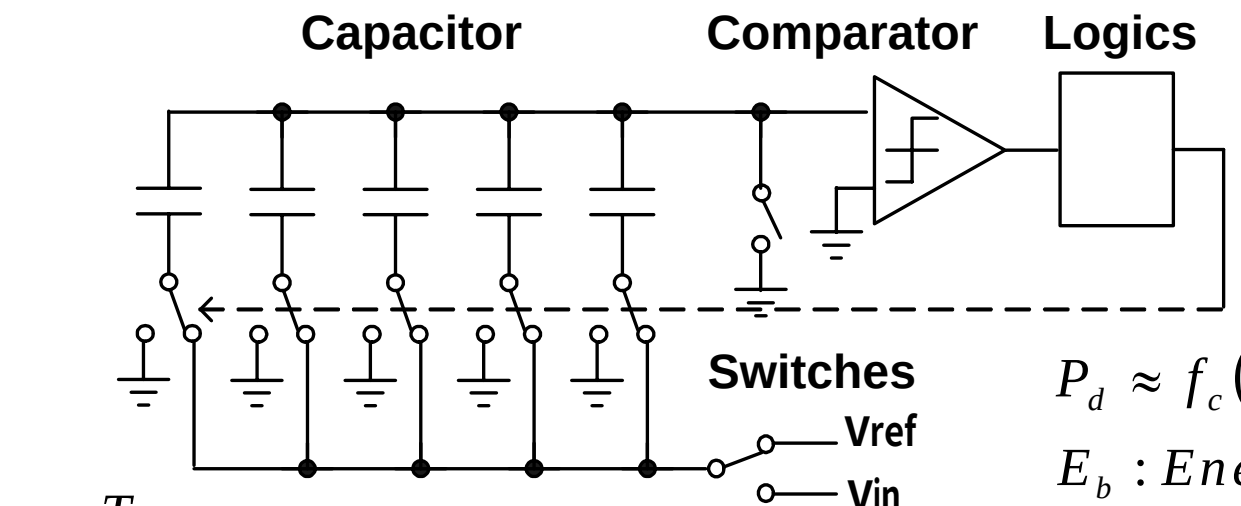
Comparator determines performance

No static current flows

SA ADC

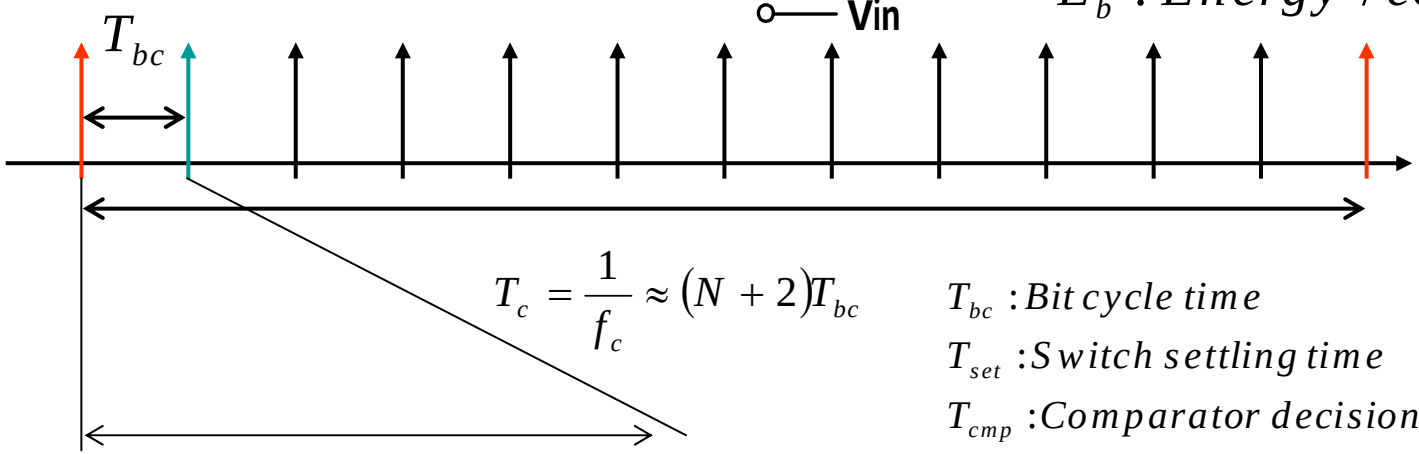
Speed of SA ADC is determined by speed of switches, comparators, and logics.

Basically independent of static current.



$$P_d \approx f_c (N+2) E_b$$

$$E_b : Energy\ /conv$$



$$T_c = \frac{1}{f_c} \approx (N+2) T_{bc}$$

$$T_{bc} = T_{set} + T_{cmp} + T_{dig}$$

T_{bc} : Bit cycle time

T_{set} : Switch settling time

T_{cmp} : Comparator decision time

T_{dig} : Logic delay time

Performance overview of SA ADCs

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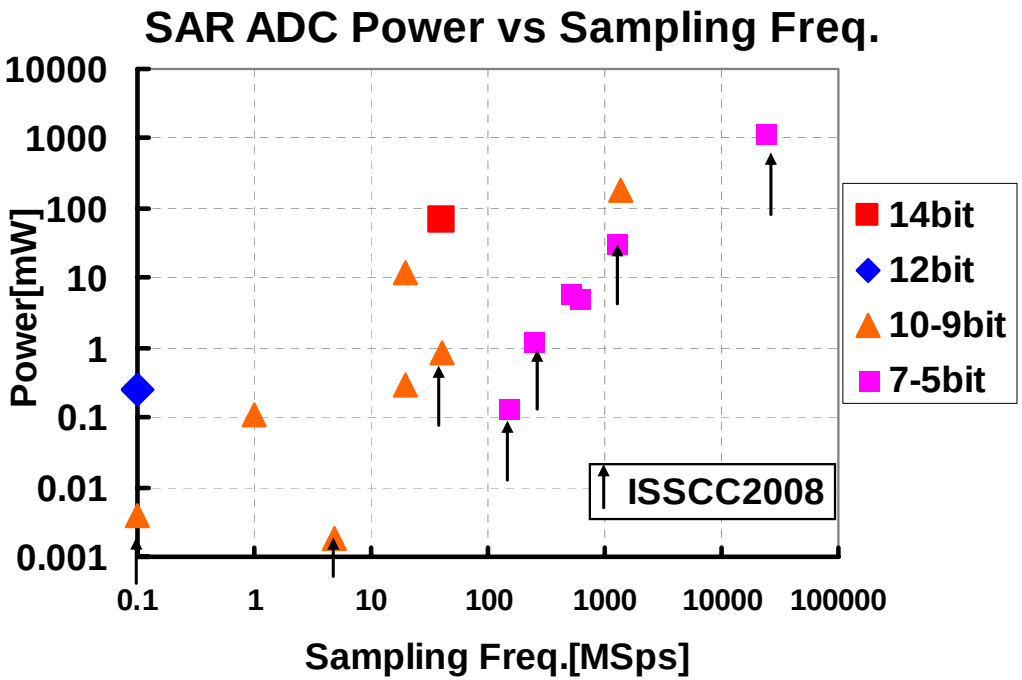
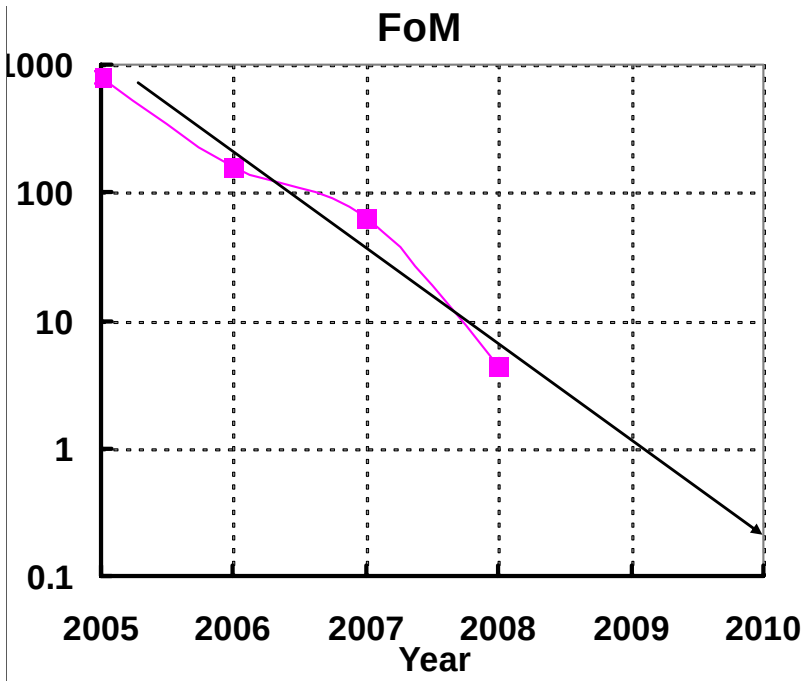
SA ADCs become dominant in every performance range.
In particular FoM has rapidly lowered.

FoM: 1/200 during past three years.

$$FoM = \frac{P_d}{f_c \times 2^{ENOB}}$$





Courtesy Y. Kuramochi

Progress of CMOS Comparator

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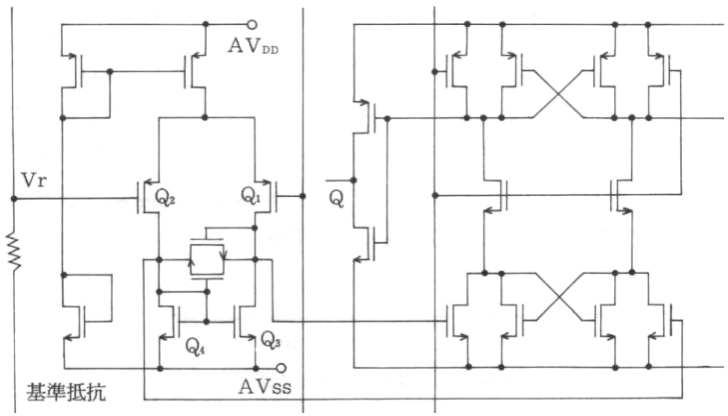
Small size MOS can be used for small mismatch circuits owing to analog compensation, however static current flows.



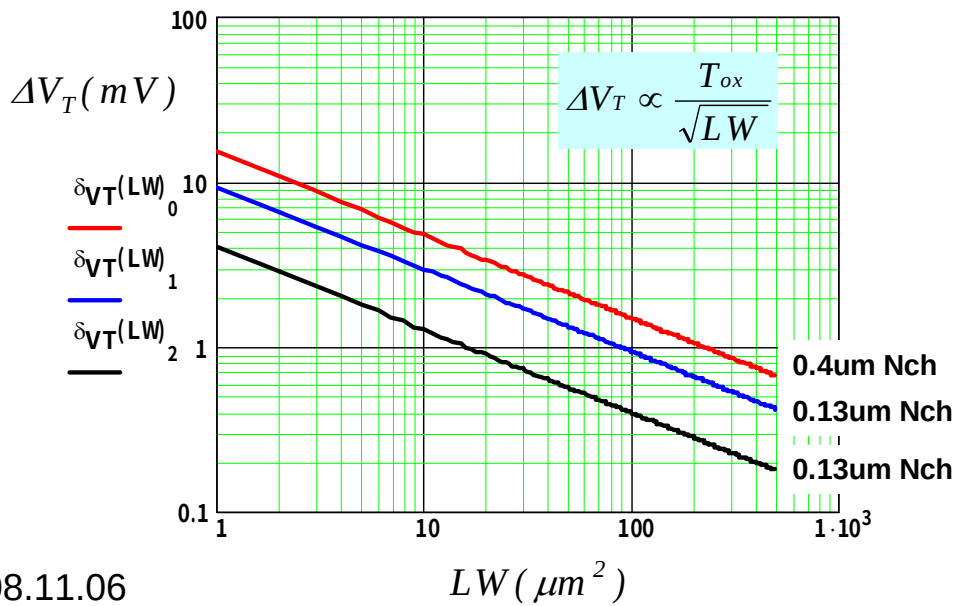
Trade off

Small mismatch ⟺ **Small area, Low power, High speed**

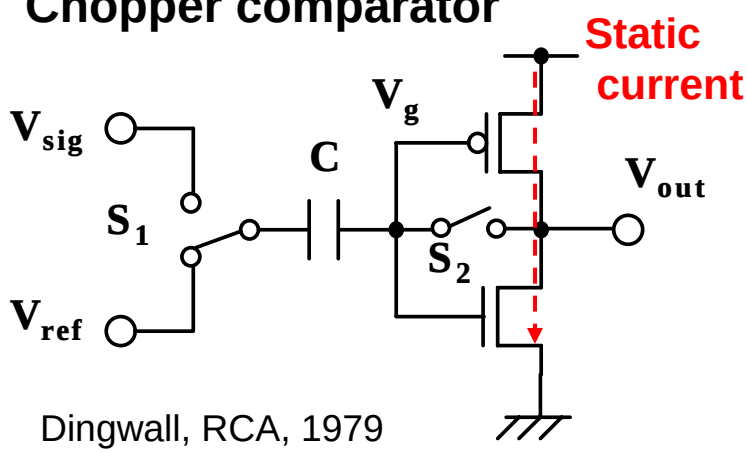
Chopper comparator solved this problem

Yukawa, et al., JSC, 1986.

Mismatch vs. gate size



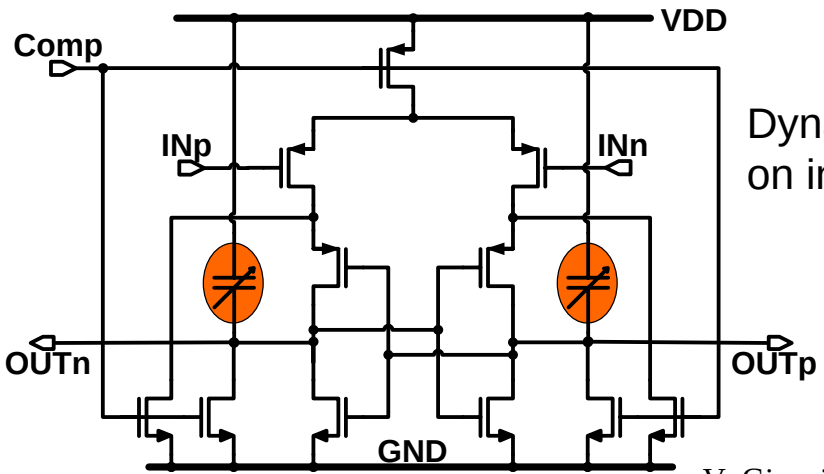
Chopper comparator

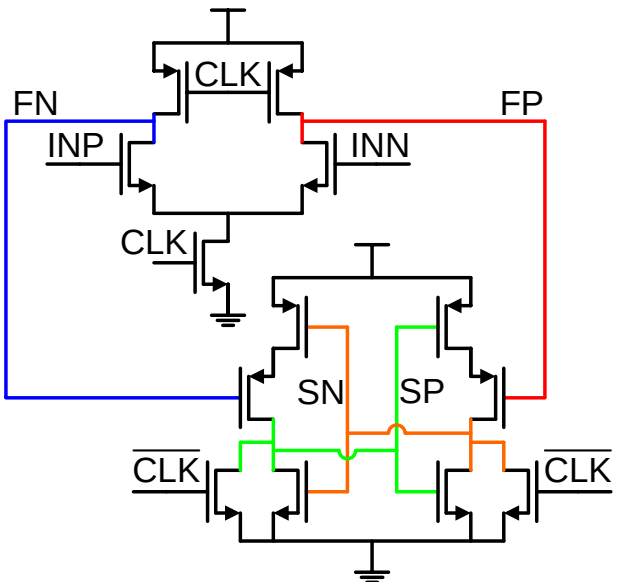


Dingwall, RCA, 1979

Recent dynamic comparators

Dynamic comparator can cut of the static current, however analog compensation is difficult to use.





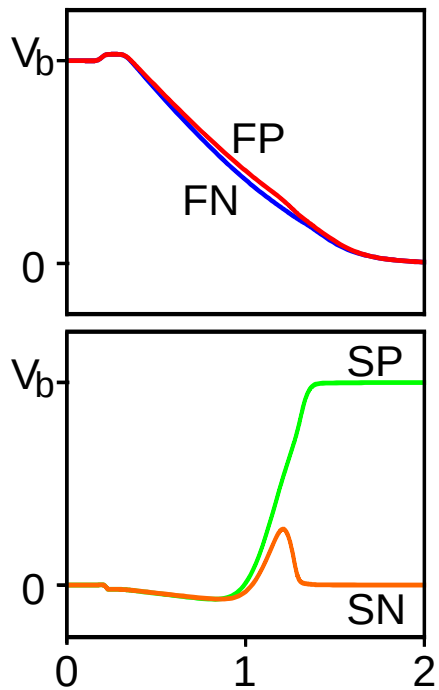
FoM can be reduced

Dynamic comparators use the fast voltage fall depended on input voltage difference

V. Giannini, P. Nuzzo, V. Chironi, A. Baschirotto, G. van der Plas, and J. Craninckx, "An 820uW 9b 40MS/s Noise Tolerant Dynamic-SAR ADC in 90nm Digital CMOS," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.238-239, Feb. 2008.

M. van Elzakker, Ed van Tujil, P. Geraedts, D. Schinkel, E. Klumperink, B.Nauta, "A 1.9uW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC," IEEE ISSCC 2008, Dig. of Tech. Papers, pp.244-245, Feb. 2008.

Fast voltage fall



Mismatch compensation for dynamic comparator

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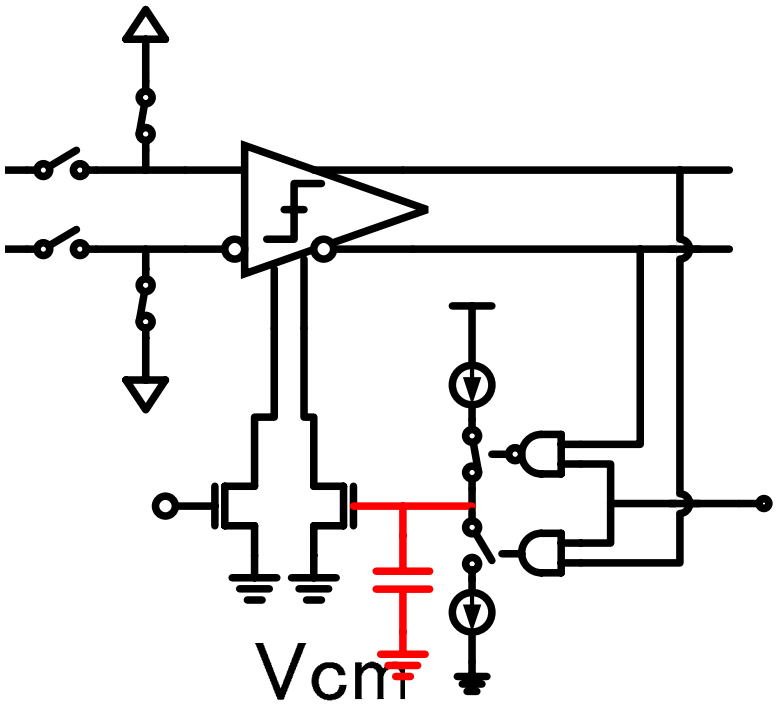
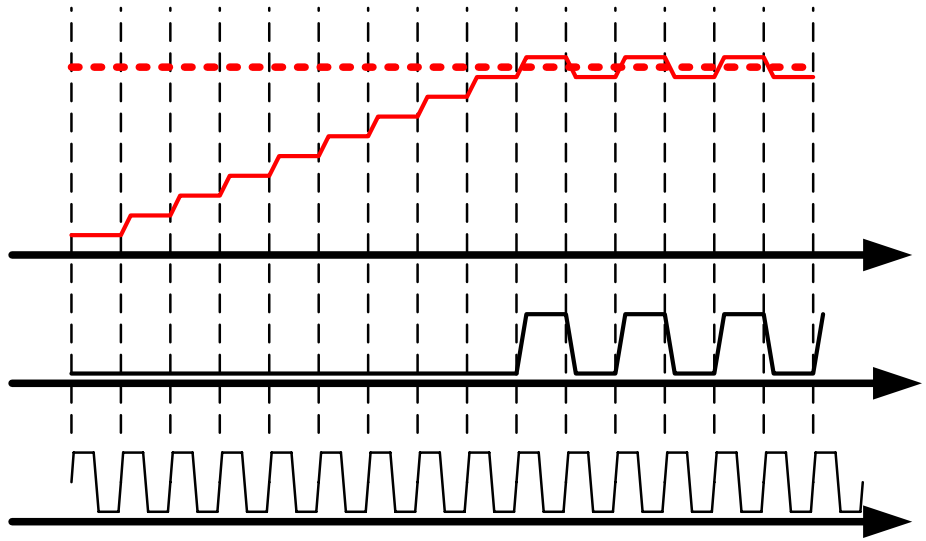
We developed mismatch compensation technique for dynamic comparator by using charge pump circuit.

Feedback loop become stable when mismatch reaches zero.





M. Miyahara, Y. Asada, D. paik, and A. Matsuzawa
A-SSCC 2008

Effect of digital mismatch compensation

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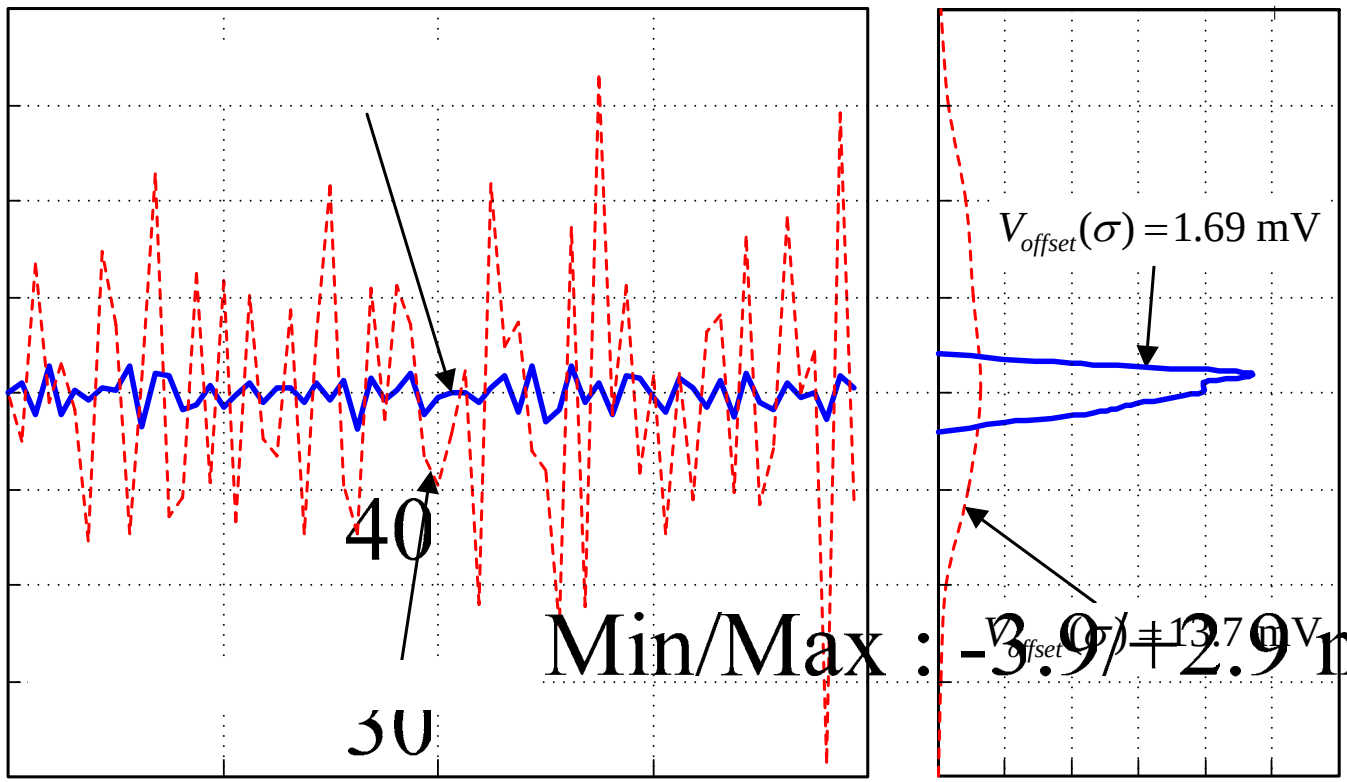
Mismatch voltage successfully reduced from 13.7 mV to 1.69mV @sigma

M. Miyahara, Y. Asada, D. paik, and A. Matsuzawa
A-SSCC 2008



Small sized SA ADC

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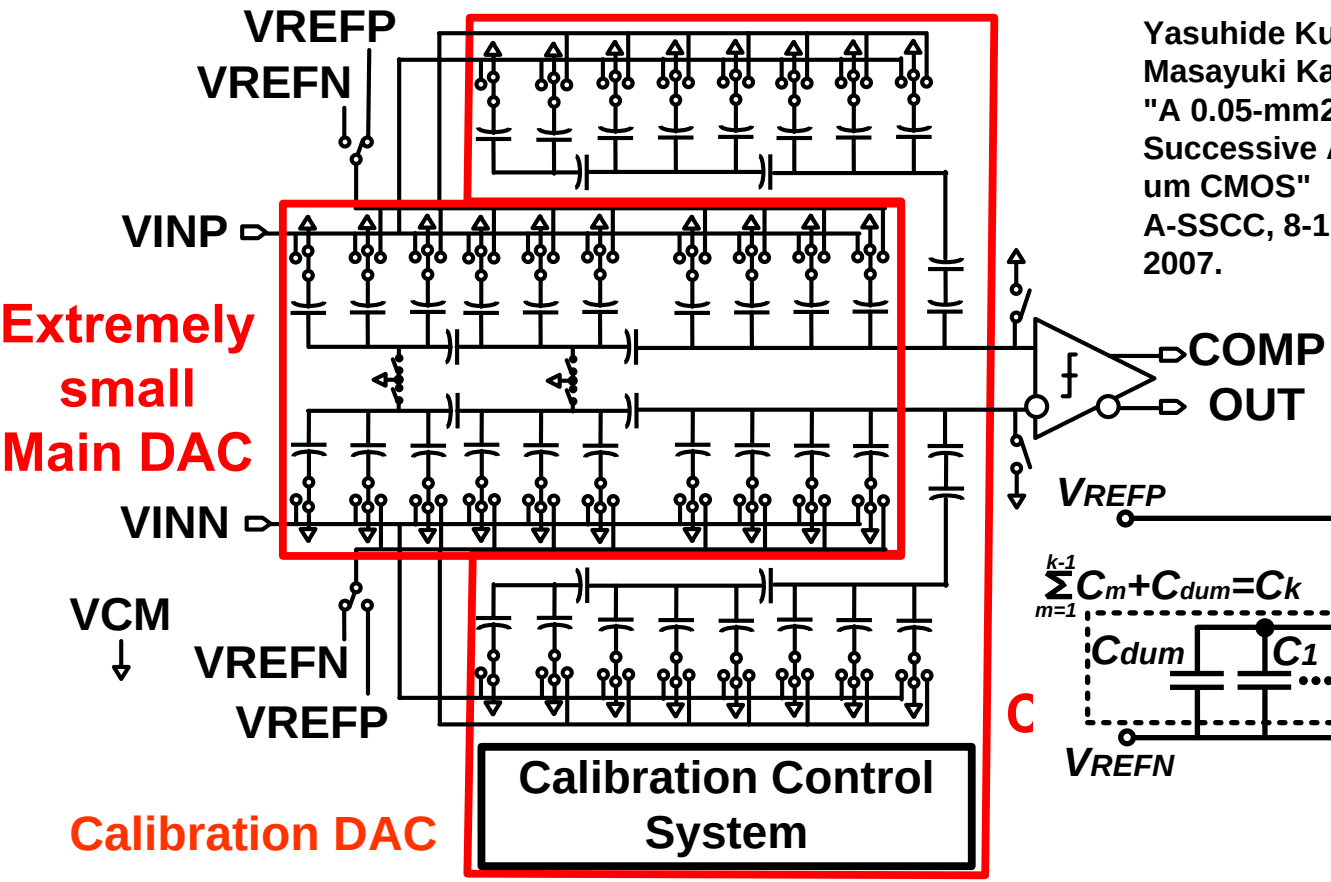
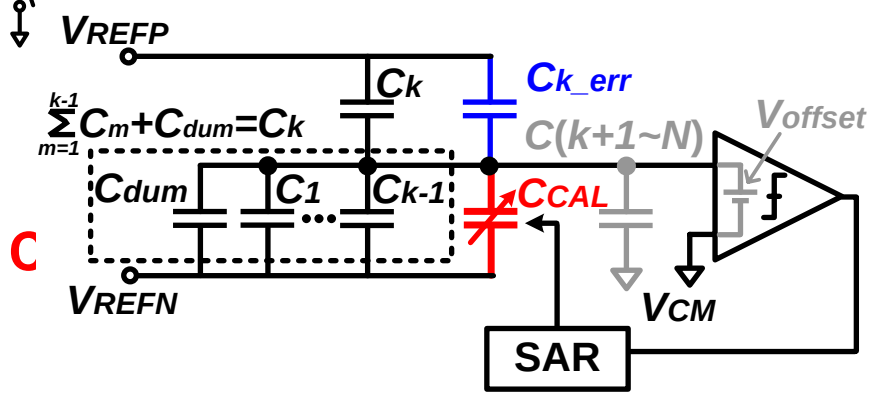
One issue of current SAR is not small occupied area.
This is due to large capacitance ratio; $C_{MSB}/C_{LSB}=2^N$
Serial capacitors can reduce this ratio,
however parasitic capacitors degrade accuracy. We solved it by calibration.



Yasuhide Kuramochi, Akira Matsuzawa, and Masayuki Kawabata
"A 0.05-mm2 110-uW 10-b Self-Calibrating Successive Approximation ADC Core in 0.18-um CMOS"
A-SSCC, 8-1, pp 224-227, Korea, Jeju, Nov, 2007.



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Effect of digital calibration

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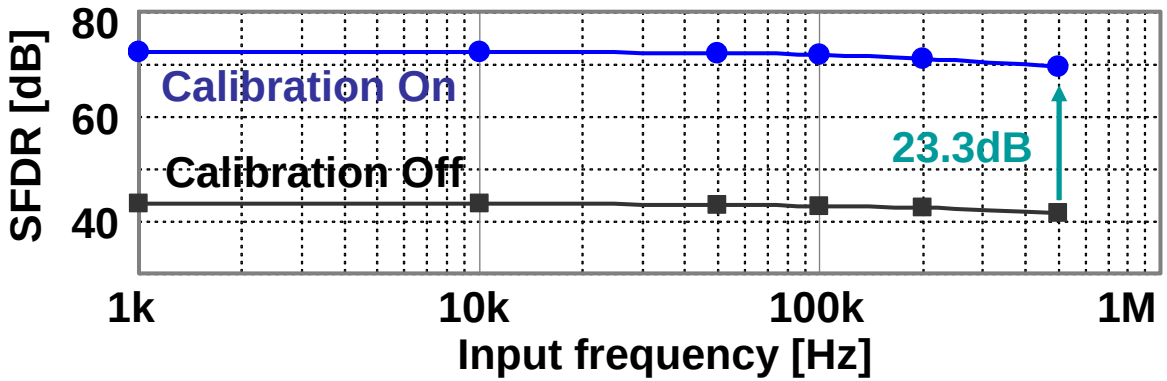
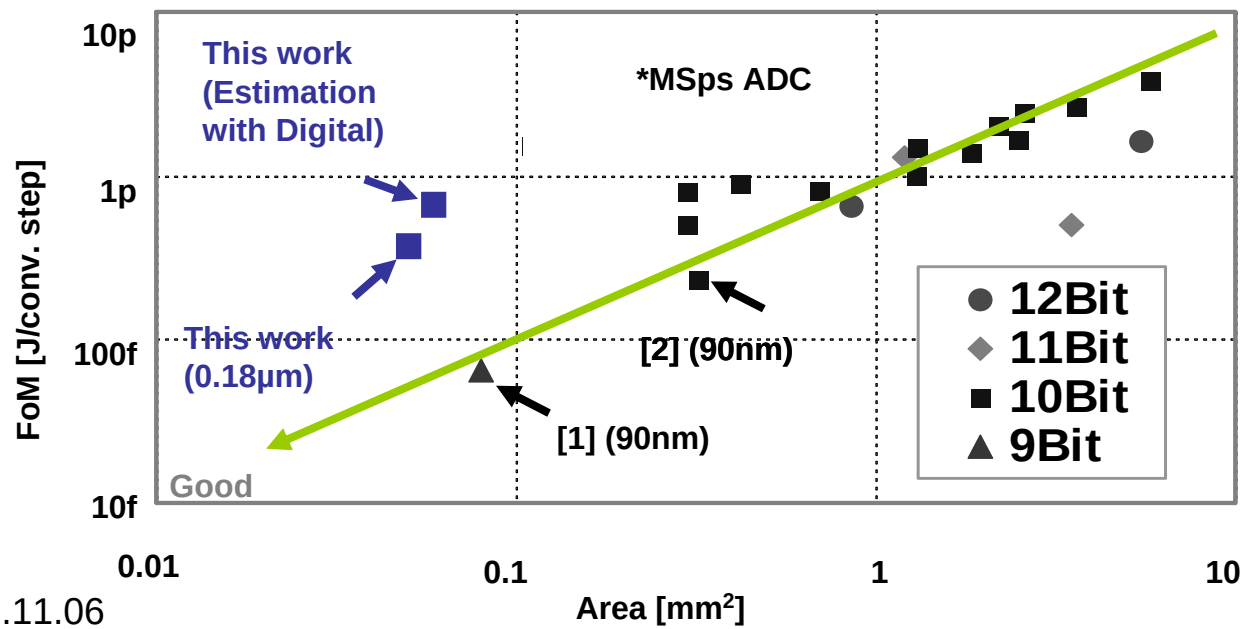
We can realize 10b ADC with high SFDR of 72dB ADC in world smallest chip size, by using digital calibration technique.



[1] J. Craninckx, et. al. *ISSCC 2007*
[2] Y. Jeon, et. al., *ISSCC 2007*



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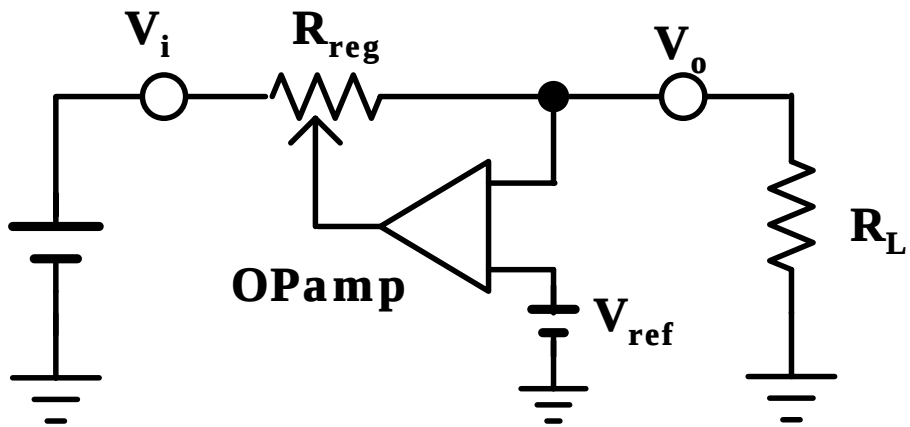
Analog vs. Digital

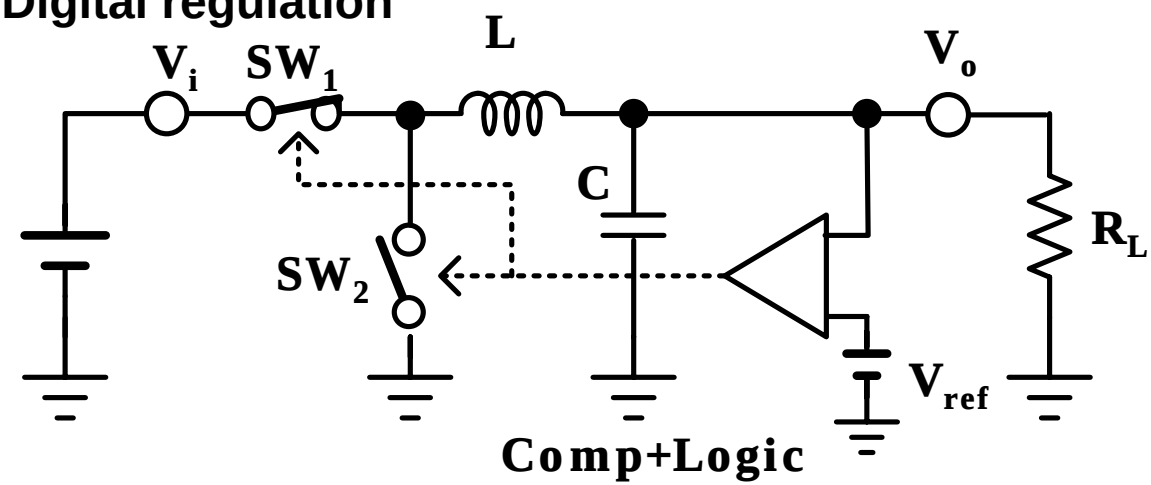
Digital (ON, OFF) control can realize lossless conversion.

Analog regulation



Clean voltage,
but low efficiency

Digital regulation



Noisy,
but high efficiency

DC/DC converter
Polar modulator

Ideally efficiency of 100% can be realized

Δ Σ modulation

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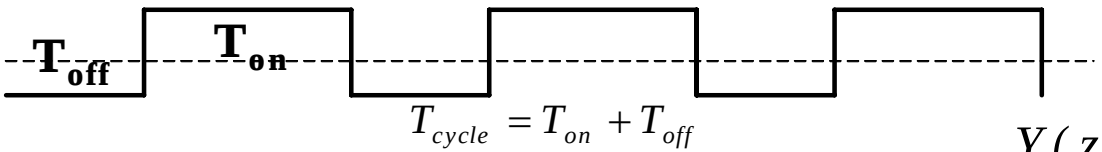
Delta-Sigma modulation method can generate average value without low frequency noise and large super tones.
High frequency noise can be suppressed by filter.

Pulse width control **Issues: Large Super tones (Fixed frequency spectrums)**

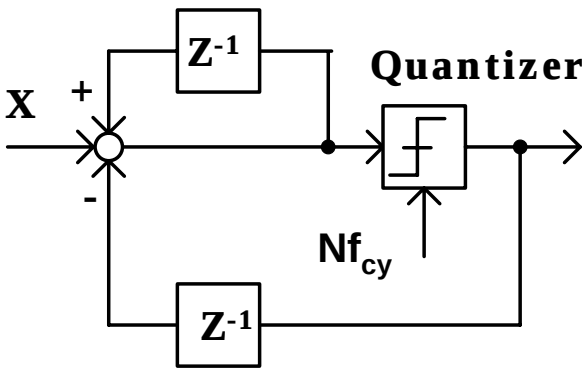


$$T_{cycle} = T_{on} + T_{off}$$

$$V_o = V_i \frac{T_{on}}{T_{cycle}}$$

$$Y(z) = X(z) + \left(1 - z^{-1}\right)^L Q(z)$$

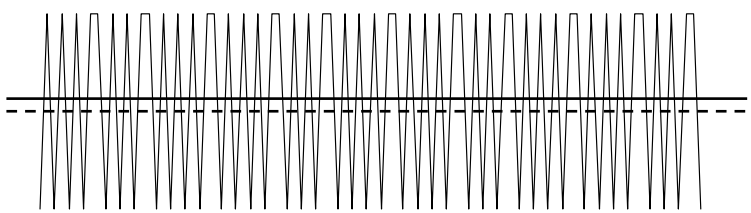
Δ Σ modulator **Lowe frequency noise is suppressed**



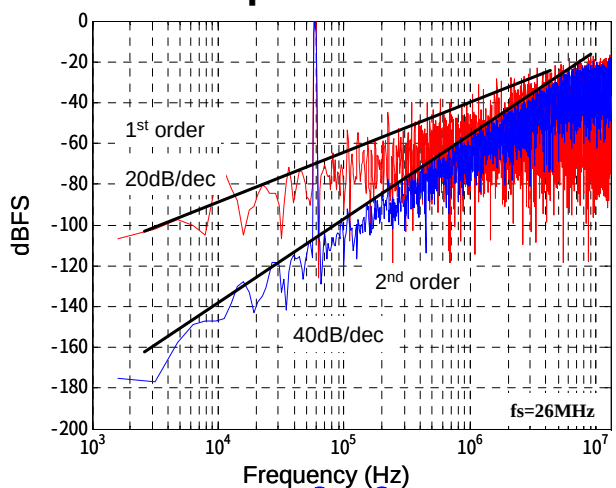
(1, 0, 0, 0, 1, 0, 0, 1, 1,...)

$$f_{cy} = \frac{1}{T_{cycle}} =$$

Output



Noise spectrum



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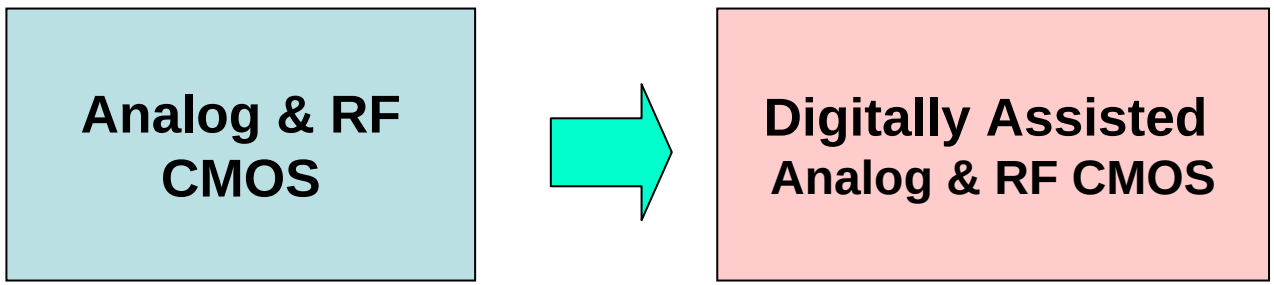
From analog centric RF to digitally assisted RF

Digital is more stable, robust, and programmable

Example: Tuner

Technology trend in RF-CMOS LSI

Analog & RF CMOS will be replaced by digitally assisted analog &RF CMOS. High performance, low cost, stable and robust circuits, no or less external components, no adjustment points, and high testability are the keys. DSP and ADC will play important roles.



Signal processing	**Analog circuits Analog processing +External component**	**DSP+ADC + Small and robust analog ckts.**
Adjustment	**External**	**Digital on chip, no external**
External components	**Large #**	**No or less**

For example: AM/ FM tuner

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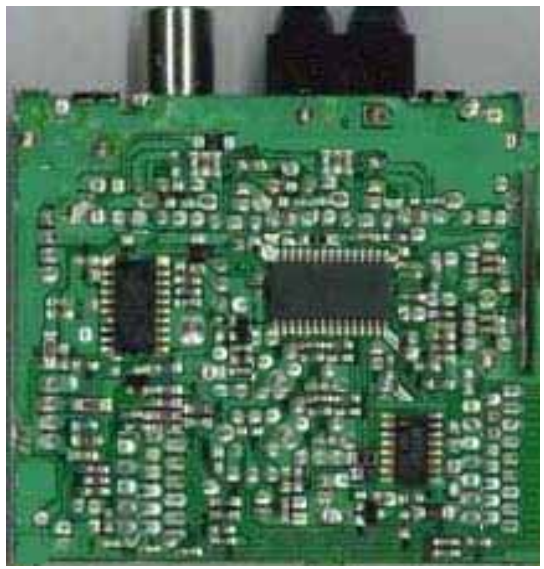
Current AM/FM tuner uses 3 ICs and large # of external components. Furthermore 12 adjustment points are needed.

Large # of products, but not expensive product.
More efforts to reduce the cost are still required.

Courtesy Niigata Seimitsu



Bipolar IC = 1 (RF)
CMOS IC = 2 (PLL, RDS)
External Components=187

AM/FM Tuner for home use
12 adjustment points

Analog-centric vs. digitally assisted

Digitally assisted RF-CMOS tuner can provide user merits.

Very small # of external components and no adjustment points.

Analog & RF CMOS technology

External components 187→ 69

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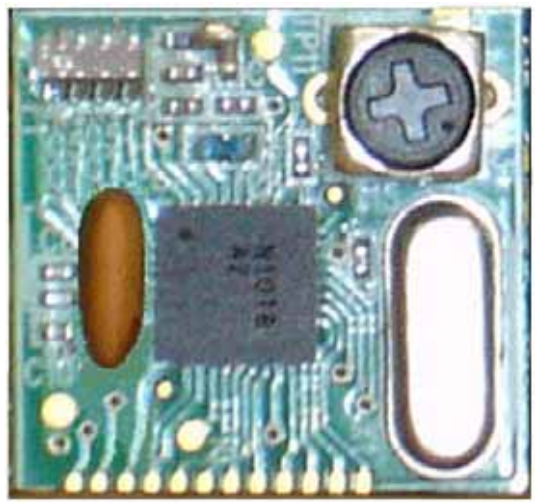
Digitally assisted
Analog & RF CMOS technology



# of external components are 11

No adjustment points

Analog-centric RF CMOS tuner

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1st trial to realize AM/FM tuner by analog-centric RFCMOS technology

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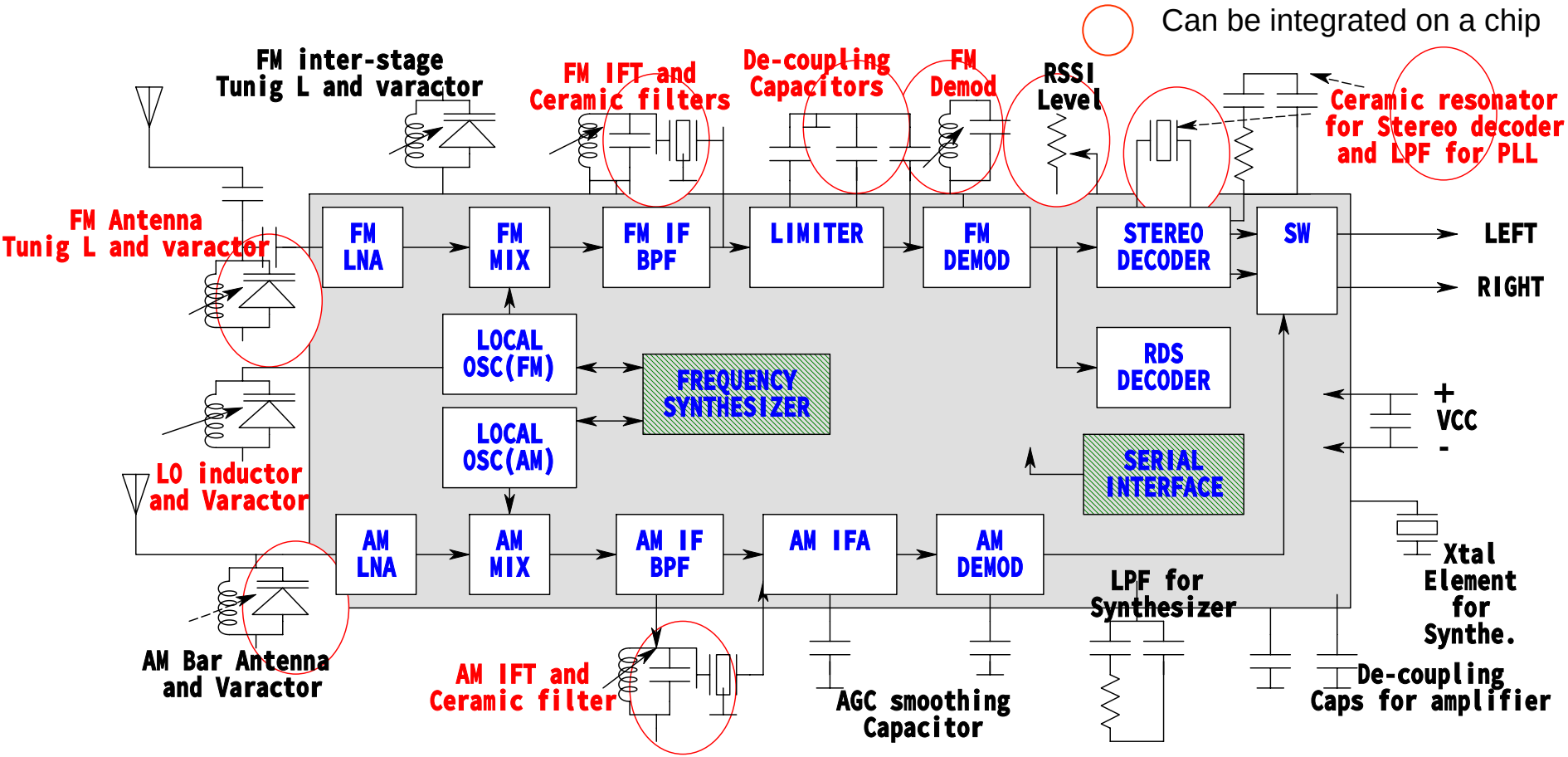
Can be integrated on a chip



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Analog-centric CMOS tuner technology

1st trial used analog-centric CMOS tuner technology.

External circuits have been replaced by CMOS, however still use analog. Thus it had many issues and many external components were still needed.

Parts	Methods for on-chip	Problems
AM/FM IF BPF	1. Low IF(a few hundred KHz) 2.Gm-C BPF with auto alignment, SCF	1.poor selectivity(-45dB), 2. SCF Switch noise 3. Center frequency shift by DC offset 4. Poor image rejection ratio (25 to 35dB)
FM Demodulator	Pulse count FM detector	Poor THD (0.5%)
Stereo Decoder	Multi-vibrator VCO, SCF filter	Large variation of free-run frequency Still need external LPF for PLL
RSSI Level adj.	Signal detector with DC compensation	Can't cover all process corner
Varactor	MOS varactor	Too much sharp C-V curve, distorted signal
AGC smoother	Time division charge and discharge	Needs large capacitor for low audio frequency
Capacitors	Stages Direct connection, use small value coupling capacitor	High impedance required, Difficult for low frequency

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Digitally assisted CMOS tuner

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Digitally assisted CMOS tuner has been developed.

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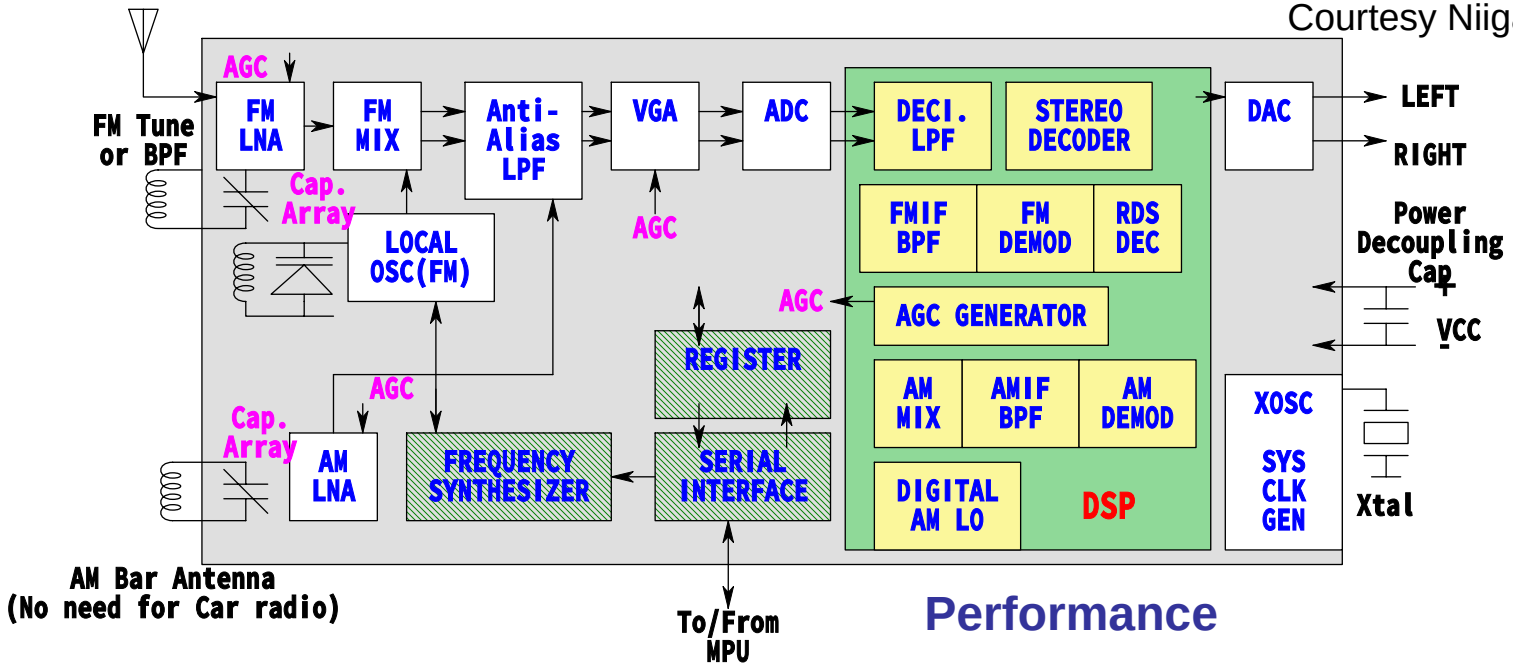


DSP realizes

1. AM/FM demodulations
2. Stereo decoder
3. AM mixer
4. Channel select filter
5. Support for image reject
6. Watch the signal revel and control gain of each stage
7. Parameter control and adjustment with MCU

Performance

Sensitivity: FM: 9dBuV, AM: 16dBuV
Selectivity: FM/AM >65dB
SNR: FM: 63dB, AM: 53dB
Stereo sep: 55dB
Image ratio: FM: 65dB, AM: Infinity
Distortion: FM: 0.09%, AM=0.25%

Image rejection in low IF receiver

Image signal can be rejected by using I/Q mixer and phase shift.

Image can be rejected theoretically, however,…

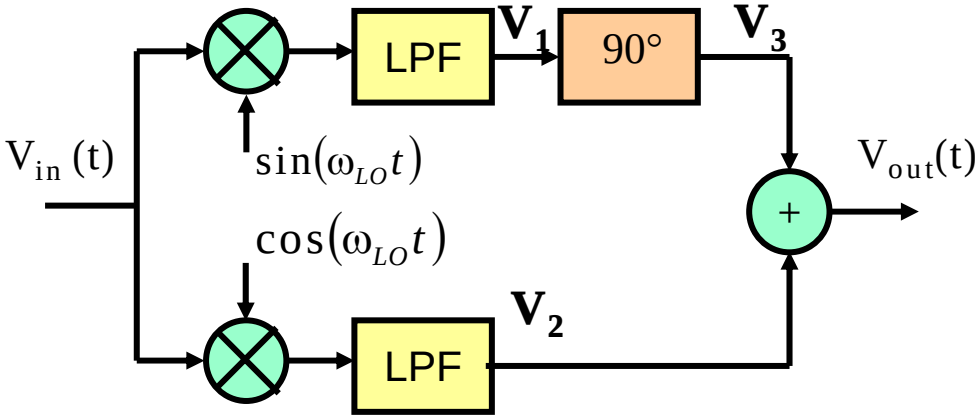
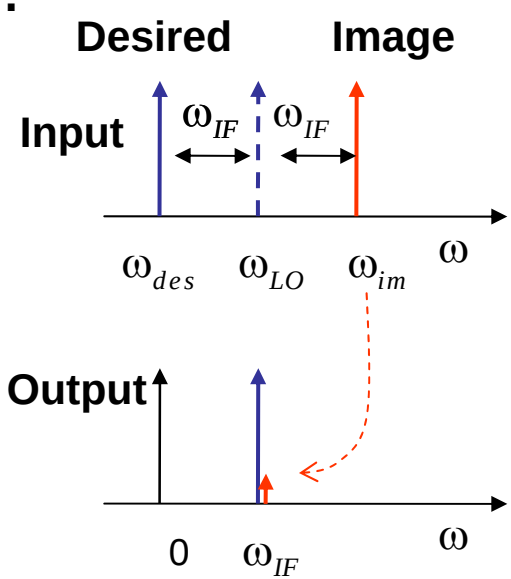


Image rejection mixer



$$V_1(t) = -\frac{V_{des}}{2}\sin(\omega_{des} - \omega_{LO})t + \frac{V_{im}}{2}\sin(\omega_{LO} - \omega_{im})t$$

$$V_2(t) = \frac{V_{des}}{2}\cos(\omega_{des} - \omega_{LO})t + \frac{V_{im}}{2}\cos(\omega_{LO} - \omega_{im})t$$

$$V_1(t) \rightarrow 90°\ shift = V_3(t) = \frac{V_{des}}{2}\cos(\omega_{des} - \omega_{LO})t - \frac{V_{im}}{2}\cos(\omega_{LO} - \omega_{im})t$$

$$V_{out}(t) = V_{des}\cos(\omega_{des} - \omega_{LO})t$$

Required gain and phase mismatch

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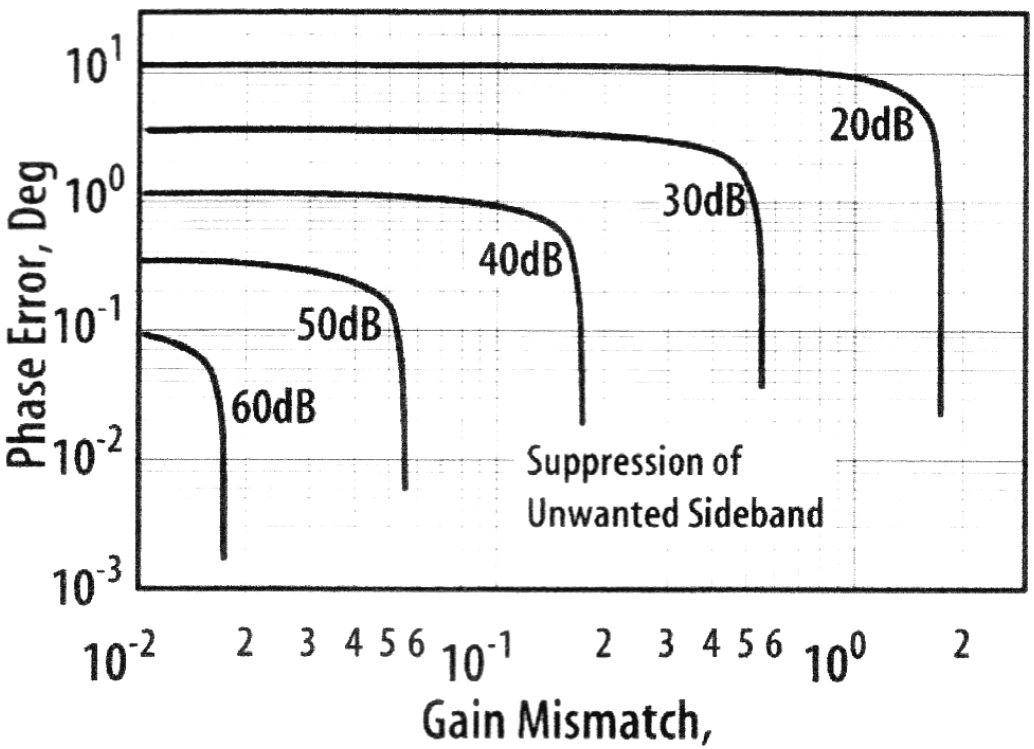
0.1 deg and 0.01% are needed for IRR of 60dB and very difficult to attain by analog technology.

IRR: Image rejection ratio



Conventional IRR: 35dB

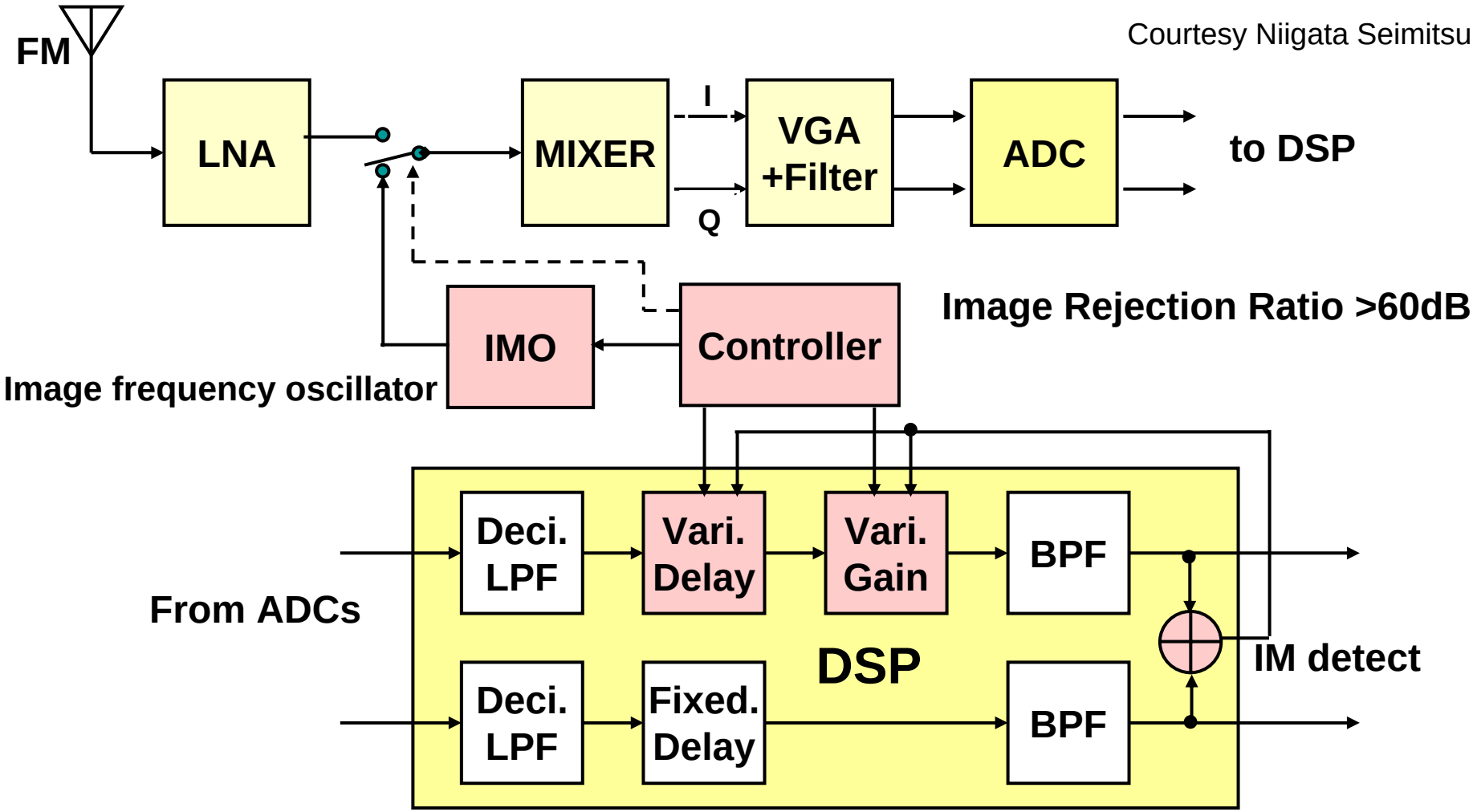
$$IRR \approx \frac{\left(\frac{\Delta G}{G}\right)^2 + (\Delta\theta)^2}{4}$$

A. Rofougaran, et al.,
IEEE J.S.C. Vol.33, No.4,
April 1998. PP. 515-534.

Digital image rejection

The dummy image signal is generated by IMO and the controller controls signal delay and amplitude on Q path to minimize the I/Q imbalance.

Courtesy Niigata Seimitsu



Summary

- **Analog has serious tradeoffs**
  - **area, cost, mismatch, power consumption, and response**
- **Analog consumes static power**
  - **OPamp-base→ Comparator-base**
- **Analog is weak in robustness and programmability**
- **Digital assistance can solve these analog issues and will be inevitable and reasonable with technology scaling.**
- **Analog and RF circuit design will make great advance assisted by digital technology.**